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Smart Microplates: Integration of Photodiode within Micromachined Silicon Pyramidal Cavity for Detecting Chemiluminescent Reactions and Methodology of Passive RFID-type Readout

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by

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Dedication

To my parents, for their love and support

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My love Jenny, you were my motivation, and I love you very much. I am so sorry.

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Since the late 1990s our group has been working with groups in chemistry department at the University of Texas at Austin on a project referred as "Electronic Taste Chip," a MicroElectroMechanical System (MEMS) based miniaturized microfluidic chemical sensor with multianalyte detection capabilities. By integrating optical detection mechanism directly onto the silicon chip a cost effective, compact, and portable sensor can be realized enabling use of these chips out of conventional laboratory environment. Addition to the integration a noble approach of accessing a photodiode with non-contact powerless RFID type readout is presented. By doing so a packaged photodiode can be interrogated without direct electrical contact, enhancing the portability even further for a sensor operated in aqueous medium. First background information regarding the project as well as design and integration criteria is presented followed by demonstration of non-

contact RFID-type readout of a photodiode. Detailed discussion on the development of process integration scheme is discussed along with the measurements verifying the performance of the fabricated photodiode. During this investigation normally overlooked design criteria of collection efficiency, the effect of how a target element is to be delivered to a detection mechanism on the overall performance of the sensor, is addressed and discussed.

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Chapter 1: Introduction

MEMS (MicroElectroMechanical System) is an art of fabricating mechanical components utilizing traditional and non-traditional semiconductor fabrication techniques, and by doing so it is possible to fabricate both mechanical components and electrical components side by side on a single substrate. The definition has broadened up to include various fabrication techniques that are irrelevant to semiconductor fabrication. Some of the commercially successful MEMS based devices which found their ways into our daily lives are DMD (Digital Micromirror Device) made by Texas Instrument which is the core placed in every TV and projectors with DLP (Digital Light Processing) signature on them, simple mechanical nozzles on a cartridge of inkjet printers made by companies such as Epson, and accelerometer made by companies such as Analog Devices detecting sudden changes of acceleration on an automobile to deploy airbags in an accident.

As shown by the last example one area that benefits from the art is sensor technology. By incorporating a mechanical structure/component right next to or on top of electronics, miniature versions of existing sensors are created with reduced cost and with much wider application resulting from its portability. Since the late 90s, our group has been collaborating with the others in the chemistry department at the University of Texas at Austin on a project to develop a new "Electronic Taste Chip" utilizing bulk silicon micromachining, a MEMS technology. This concept for analyzing multiple analytes in a complex fluid was initially reported in 1998 [1.1]. This system utilizes polystyrene-poly (ethylene glycol PS_PEG) micro-spheres, which have diameters of ~130μm when dry and ~230μm when wet, and agarose beads with sizes ranging from 250μm to 350μm. These chemically derivatized microbeads are immobilized within silicon pyramidal

cavities fabricated by anisotropic KOH etching in an array format, typically 4x5 to 5x7 in size. This silicon platform is housed within gasket layers made out of clear acrylic to provide liquid sealing and external fluidic connections. The analyte is introduced to the silicon chip via flexible tubing connected to the gasket layers from the top, reacts with the microbeads, and is extracted through the bottom. External illumination (in the laboratory version, a mercury arc lamp with a band-pass filter) is applied on one side of the chip, and the fluorescent signal is observed by a CCD (charge coupled device) camera, which is mounted along with an optical microscope. The visual information (spectral change) is then analyzed, and "both fluorometric (based on epifluorescence data) and colorimetric (based on transmission data) procedures are used to quantify analyte concentration" [1.2]. Figure 1 (a) shows an SEM (Scanning Electron Microscope) picture of an array of the micromachined cavities with beads placed in them, and Figure 1 (b) shows the schematic of the current detection methodology. Information about the analytes that are currently detectable via the "Electronic Taste Chip" can be found in previous publications such as references [1.1] to [1.4].

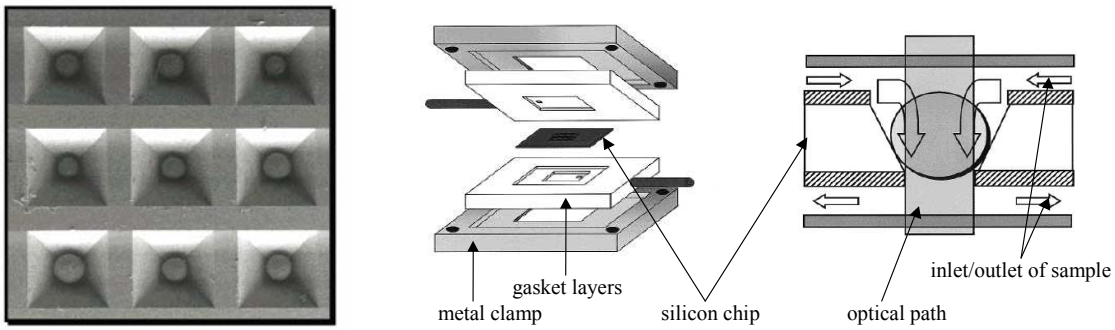

Figure 1.1: (a) SEM picture of an array of micromachined cavities with chemically derivitized microbeads placed within the cavities; (b) illustration of the current operation setup for the "Electronic Taste Chips."

These liquid phase, multi-analyte detector arrays already have demonstrated an impressive range of detection capabilities, including pH, metal cation, cardiac risk factor, and DNA oligonucleotides. However all the current detection chemistries are based on colorimetric or fluorescence detection; fluorescence detection in particular requires a UV (Ultra Violet) excitation source as well as a CCD camera to capture the fluorescent signal. Figure 1.2 shows a picture of the current lab station for making fluorescent measurements.

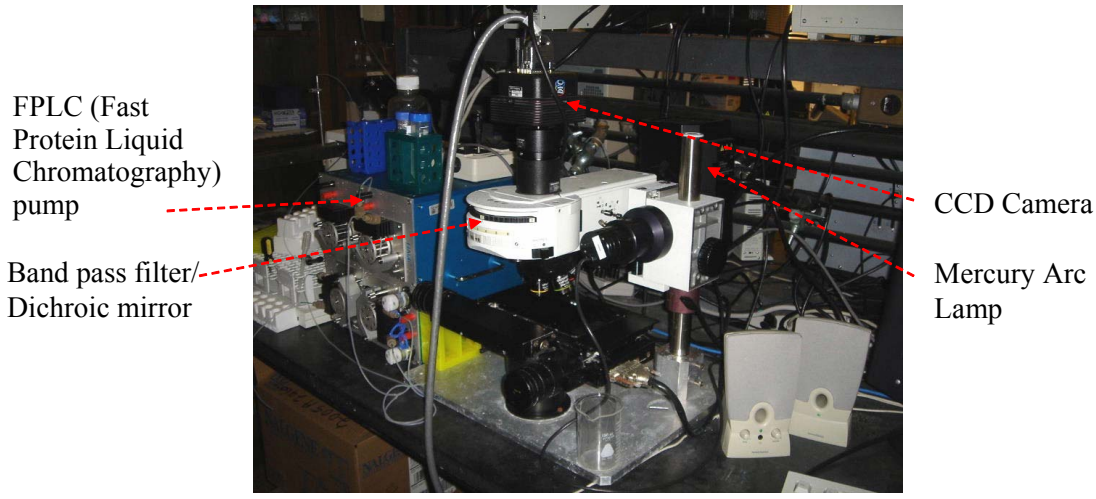

Figure 1.2: Picture of the current lab station for making fluorescent measurement, taken from Mcdevitt Research Lab at the University of Texas at Austin.

In this dissertation an evolved version of the electronic taste chip based on chemiluminescence to detect analytes is presented. Chemiluminescence is "chemical reactions which emit light," in simple terms [1.5]. Therefore by changing the chemical detection scheme from fluorescence to chemiluminescence, the UV excitation source would be no longer required. And by integrating detecting electronics directly into each cavity, which is the main topic of this dissertation, the collection optics can also be

eliminated. This miniaturized system could then be used more easily away from the traditional laboratory settings, a paramount advantage in many situations for a sensor.

It is no secret that conceptually similar microfluidic/lab-on-a-chip type sensors are actively being researched throughout the world. However, one practical aspect that is not emphasized in many of the sensors is how a target is to be delivered to the detector, the collection efficiency. Typically a photodiode used in optical communication system is developed to detect collimated light signal; hence, the detector is fabricated on a planar surface with assumption of specific angle of incidence, and the collection efficiency, in this case the external quantum efficiency, would solely depend on the performance of AR (Anti-Reflection) coating as the light is focused/guided directly to the photodiode by external optics. On the other hand if the target is not a controlled source, i.e. collimated light, the collection efficiency should be an integral part of the design and development.

For example, there are numerous detectors that are very sensitive such as single photon detectors. For the sake of argument let the area of the photodiode be as small as a photon. If the fabrication technology enables creation of such minute detector and if the detector is sensitive enough to detect a single photon, it would be a quite of an accomplishment. However, another integral question that should be asked is how would that single photon find its way to the detector in a given environment? If a detector is sensitive enough to detect a molecule, the sensor would be regarded as very sensitive, but again how would a molecule find its way to the sensor? What efforts would be required to ensure that the molecule will find its way to the detector? If the area of a detector is increase by a factor of 10, the noise surely would increase at a similar rate. Should the detector be regarded as 10 times less sensitive even if the probability of a photon/molecule finding the detector has just gone up by a factor of 10? All these questions are intriguing and complex by nature, and we hope to get a glimpse of the

answers during the course of development of the integrated photodiodes within silicon pyramidal cavities for detecting chemiluminescent reaction.

Addition to the fabrication of the MEMS based sensor, a new methodology of remotely accessing photodiodes by wireless inductive coupling similar to EAS (Electronic Article Surveillance) tags is presented. In the past, our group has been working with the civil engineering department at the University of Texas at Austin developing wireless sensors utilizing EAS tags for the purpose of structural health monitoring [1.5, 1.6]. The goal of this research project was to develop an inexpensive and reliable structural health monitoring sensor that could be interrogated after an earthquake, for example, with minimal disruption to the normal activities within the building. Figure 1.3 shows an illustration of this concept. Although the wireless scheme was devised to meet the constraints of civil engineering applications, similar approach can be useful for a chemical sensor as one significant challenge for micro-total analytical systems (μTAS) is integration of many microfluidic components in a manner that does not interfere with electrical or optical access to the actual transducer.

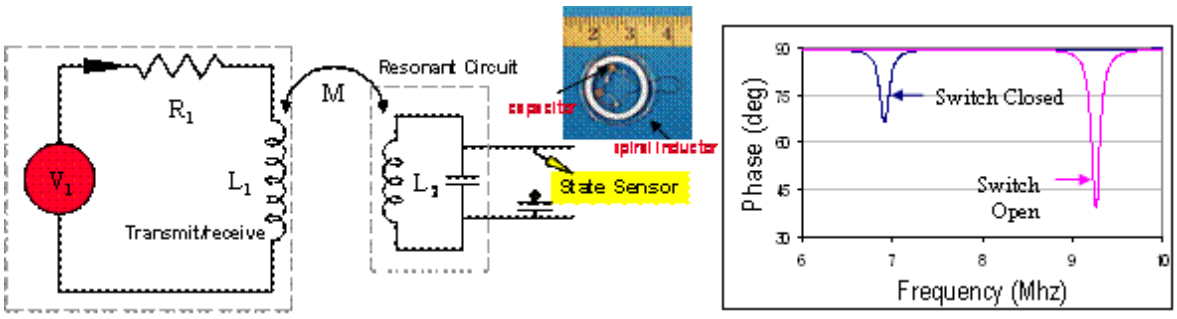

Figure 1.3: Electronic structural surveillance tag that allows wireless, remote monitoring of damage in civil structures such as welded steel frames or reinforced concrete [1.5].

In chapter 2 background information regarding the project is introduced. First a literature review on some of the photo detectors detecting chemiluminescence is presented followed by past works, bead confining cantilevers and AR coating with single silicon nitride layer, is presented as they are related to the project and as an example of MEMS based semiconductor fabrication. Basic design principles behind semiconductor photodiode are also discussed.

Chapter 3 deals with the preliminary experiment on demonstration of accessing a photodiode using inductive coupling. After introducing basic circuit theory regarding inductive coupling, demonstration of the idea using commercially available silicon PIN (p-intrinsic-n) photodiode is presented, and analysis of the raw data obtained from this experiment is analyzed. By doing so guide lines as to the design of such system is discussed and presented.

Chapter 4 presents various fabrication steps for integrating the photodiode in micro-machined pyramidal cavity. First two sections are dedicated to present the initially failed attempts as well as analyses on those attempts. Although these initial steps resulted in *pn* junctions with high reverse bias current they are presented as negative know-how. Additionally these steps are quite different from nominal semiconductor fabrication steps, and they could be useful for other applications. Chapter 4 also includes basic knowledge and concerns in fabricating a *pn* junction and is finished off with completed integration scheme of a *pn* junction with low reverse biased current.

Chapter 5 contains measurement and analysis of the fabricated device. One in particular quantum efficiency of the photodiode is measured. Additionally answers to the questions asked in the last page are addressed, and a rapid prototype of passive RFID-type readout of fabricated photodiode is presented.

Chapter 2: Background

2.1 CHEMILUMINESCENT DETECTION EXAMPLES

Although there are numerous solutions for optical detection, non-silicon based solutions such as Ge photodiodes are not heavily considered because the current system is based on silicon. In fact the probable reason for choosing silicon as the base material at the beginning would have been its easiness of fabricating the cavity for supporting micro-spheres (mechanical aspect) as well as the availability of matured fabrication techniques for integrating electronics such as IC's and photodiodes (electrical aspect). According to the reference [2.1, p95] the spectral response of chemiluminescent detector should be sensitive over the lights within 400*nm*~600*nm* at least. Preferably the coverage be over the entire visible spectrum, 380*nm*~750*nm*. Figure 2.1 is a generic graph of the absorption (m^{-1}) versus wavelength (μm) for various semiconductors with indirect bandgap adopted from reference [2.2].

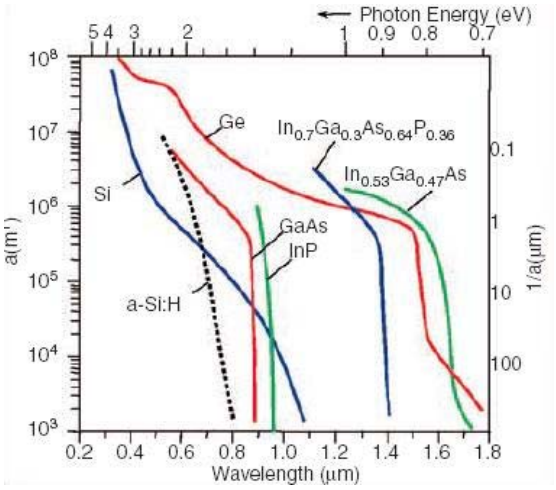

Figure 2.1: graph of absorption vs. wavelength for various semiconductors [2.2].

From the figure silicon is clearly sensitive up to 1100*nm* region, and additionally the steepness of the absorption coefficient curve within the visible spectrum can be advantageous in terms of wavelength selectivity. For example one group demonstrated a silicon color sensor, which is a tighter constraint compared to detecting presence of light regardless of the wavelength, based on the wavelength dependent response of reverse biased photodiodes [2.3]. This group strategically fabricated two photodiodes (*p*-substrate, *n*-epilayer, and *p*-implant) on top of each other; hence, the photons of different wavelengths transmit through different layers and are absorbed by different diodes strategically located at different depths. The sum and ratio of the currents generated by two diodes are used to determine the wavelength/color. Although sharp distinction of wavelength is not a heavy constraint for the proposed device, it should be considered in the case of fluorescent detection because wavelength of excitation source needs to be blocked off.

Other groups have already introduced on-chip detection method for observing chemiluminescence or bioluminescence. One team has demonstrated detecting electrogenerated chemiluminescence of Ru(bpy) at Pt electrodes with *pn* junction diode. This simple *pn* photodiode is fabricated by *n*-type diffusion on *p*-type silicon substrate (3-5 Ωcm), and there are 50 interdigitated Pt electrodes, which is 1*mm* long, 3.2μm wide, and are separated by 0.8μm gap. (Effective area of the photodiode is 0.2-0.4 mm^2) The advantage of such a system is clear: the emission of light occurs close to the electrode located directly on top of the photodiode. The paper also states that a PECVD (Plasma-Enhanced Chemical Vapor Deposition) silicon nitride layer (4000$\AA$) is deposited for electrical isolation of the diode as well as for anti-reflection coating of lights with 610nm wavelength. The peak responsivity at 610*nm* is about 0.48 $\mu A/\mu W$, and the dark current is in the scale of 100*pA*. The breakdown voltage was about -15 V [2.4].

Another team built a bioluminescent bioreporter integrated circuit that contains a double *pn* junction photodiodes (*p*-diffusion, *n*-well, and *p*-substrate) which has a quantum efficiency of ~66% at 490*nm*. The focus on this device is to investigate photo detectors fabricated within the boundary of CMOS IC process with various spectral responses. The wavelength dependent response is achieved by optical filters, which is built with a permutable combination of poly-silicon layers, gate oxide, and field oxide. Additionally it includes integrated circuit design of output signal processing, and by attaching a RF transmitter the system is claimed to be wireless microluminometer [2.5, 2.6].

There is an instance where *pn* junction based photodiode is built at the bottom of the substrate, 350μm thick FZ (Float Zone) silicon DSP (Double Side Polished) wafer with very high resistivity greater than 500Ωcm. The design is more like a huge PIN (*p*+-*intrinsic*-*n*+) photodiode where the bulk of the substrate is the intrinsic layer. The chemiluminescent light generated within the large channel engraved on the top surface is absorbed directly into the silicon substrate, and the generated carriers are collected at *p*+ and *n*+ interdigitated electrodes placed 200μm below the channel. This device detects chemiluminescent reaction involving hydrogen peroxide, luminol and a catalyst (irons). The diodes were connected to a transconductance amplifier; however, the actual performance of the individual diode was not presented [2.7].

Although an elaborate optical filter is used to suppress the excitation source of wavelength less than 500*nm*, *pn* junction based photodiode was used for fluorescence detection (515*nm*) in a DNA analysis device. This complex/comprehensive sensor contains fabricated microchannels, heaters, temperature sensors, and fluorescence detector. “This device is capable of measuring aqueous reagent and DNA-containing solutions, mixing the solutions together, amplifying or digesting the DNA to form

discrete products, and separating and detecting those products," and all of the above operations are done within the system. Specific numbers of the detection efficiency is not provided [2.8].

In this section some of the examples of on-chip chemiluminescent detectors searched/reviewed before the project has actually begun are presented. A large amount of these works on the optical detection of chemical/biological reactions has concentrated on either improving the signal processing capabilities of planar, imager-like, detectors or developing a dedicated detector for sensing one specific phenomenon at a time. In our platform photodiodes are designed to be directly integrated into micromachined cavities in an array, reminiscent of a microplate, which potentially enables multi-analyte detection capabilities.

2.2 HYBRID VERSUS INTEGRATION

Before getting into the technical aspect of the design, the validity of the integration approach is examined. As stated main motivation of this project is to miniaturize the current setup so that the sensor can potentially be used out of laboratory environment. At this time the detection mechanism involves complex/expensive optical lenses addition to the not-so-cheap CCD camera. Hence the first obvious approach is to build a miniaturized version of the current setup as shown in figure 2.2.

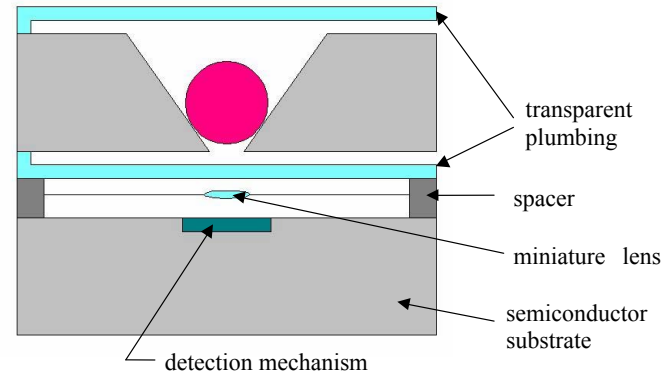

Figure 2.2: Schematic of possible hybrid model and integration model.

The notable advantage of such design would be the usage of any detection mechanism fabricated on a planar substrate not limited to silicon. In fact it would be possible to adopt commercially available photo-detectors with high performance since the substrate is to be simply attached. However other than the mentioned advantage, all the other elements of the above design are problematic. First it is not trivial to fabricate micro-lenses with controlled parameter although there are techniques available for fabricating micro-lens arrays by etching or molding glass, silicon or plastic substrates. Second, the fabricated lens array has to be attached to the detector substrate, and then the assembly needs to be attached to the silicon chip.

During the assembly, even if the issue of bonding three different substrates and spacers in between are resolved; an important aspect of such hybrid design would be 3-dimensional alignment of the lens and detector structure respect to the micro-beads unless a large imager-like detector is used to cover entire array of beads. This aspect of mechanical alignment in a MEMS hybrid system not only increases the cost but also requires careful calibration of the detectors afterwards (since the external efficiency would depend on the actual position of the lens/detector), and it limits the device density as well. It might be possible to place an array of detectors without the lenses, but the performance might be poor as the dim light generated by chemiluminescence has to go through three different mediums (an unknown liquid sample, a transparent cover, and air) before reaching the detecting substrate.

On the other hand by integrating the photo-detectors within the cavity, micro-lenses will not be required because the chemical reaction occurs right next to the detectors, all the alignments will be carried out via already established photolithography process, and the device can be fabricated monolithically, which eliminates both mechanical alignment and bonding of other substrates. Figure 2.3 shows two possible

places for integrating the detectors. For the detector located at the bottom of the substrate, the fabrication would be straight forward as the detector is built on a planner surface, but the photon would have to pass through the silicon substrate before reaching the collection site. Therefore it is unlike to be efficient unless the collecting region extend far into the substrate, i.e. substrate with high resistivity. On the other hand the detector on the sidewall would have to be built on a slope, but the collecting region should be much closer to where the chemiluminescent reaction occurs.

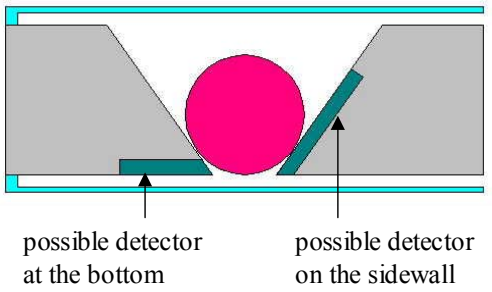

Figure 2.3: two possible integration of photodetectors.

2.3 DIFFERENT TYPES OF SILICON PHOTODETECTORS

There are several optical detectors that can be fabricated on a silicon substrate, and each of them has its own advantages and disadvantages. The following section describes the possible detectors and compares them with their adaptability to this project. One unique aspect of this sensor is that the liquid sample goes through the substrate; therefore, the photodetectors must be fabricated on a substrate with an array of openings, as shown in figure 2.3. Additionally what differentiates this device from other chemiluminescent detectors is the objective of detecting different reactions occurring within individual cavities. Once a liquid sample enters the array of cavities, each bead would react differently to the sample, and the composition of the sample is determined by observing the individual reactions to the beads with known compositions. Moreover

unlike the photodiodes used in optical communication, sensitivity and noise are more critical than response speed.

2.3.1 Schottky diodes and CCD (Charge Coupled Device)

First Schottky diode is discussed. From the viewpoint of how the photons are collected MSM (Metal-Semiconductor-Metal) diode and CCD (Charge Coupled Device) would also fall into this category. The basic operation principle is that photon enters the depletion region, created by the work function difference/bias between the metal contact and the semiconductor, and produces drift photocurrent. In the case of MSM diode two metal strips are used, and the second strip forms a forward biased Schottky diode right next to the reverse-biased diode. For the CCD, there is a silicon dioxide layer between the metal and the semiconductor for insulation. The charge is stored within the depletion region underneath the biased strip, and clocking series of metal stripes induces charges out. Figure 2.4 shows illustration of these diodes.

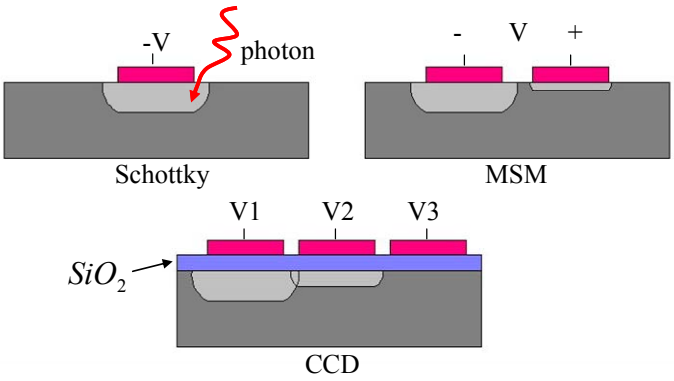

Figure 2.4: Illustration of Schottky diode, MSM diode, and CCD.

In terms of fabrication these are the simplest as only the metal with appropriate work function is needed to be deposited and patterned, but this is only true when they are built on a planar substrate. (Actually fabricating a good CCD is not a trivial task because

it requires perfect charge transfer for the read out.) In fact it would be very difficult to fabricate any type of intriguing electrodes on the sidewall as the depth of the cavity is about 250μm. Minimum feature size with a typical photolithography process (λ~400nm) for a gap of 250μm is approximately 15μm. (W_{min}~1.5$\sqrt{\lambda \cdot gap}$, equation estimating minimum feature size of proximity printing from reference [2.9]) Additionally the depletion region directly underneath the electrodes cannot collect photons due to the shadowing from the metal electrodes unless the metal layer is sufficiently thin/transparent. More practical solution would be to place the electrodes at bottom surface, but in order to have good efficiency/sensitivity, the depletion region need to extend far into the substrate as 99% of the light with the wavelength of 500nm would be absorbed within 3.84μm. (Absorption = $e^{-\partial W}$, reference [2.10].) Other than applying high bias voltage the depletion width is lengthened by using silicon substrate with high resistivity such as FZ (Float Zone) silicon wafer, but not only it increase the cost but also it may limit the device density because longer minority carrier life time/diffusion length would result in cross talks between cavities.

For example EHP (electron hole pair) generated from a photon entering a sidewall of neighboring cavity may diffuse toward the electric field generated by other electrodes. Reference [2.11] has a recorded minority carrier lifetime of 10^{-3} seconds in *p*-type silicon and 10^{-2} seconds in *n*-type silicon at room temperature with carrier concentration of ~$10^{15} cm^{-3}$. This translates into diffusion length of 1760μm and 3600μm respectively. (L = $\sqrt{(KT/q)\mu\tau}$ and other similar measured values from reference [2.12].) Although the above values are obtained with highly pure silicon, they indicate that the distance between each cavity should be at least a few millimeters! Overall, Schottky type diodes including CCD are not viable because it is impractical to fabricate them on the sidewall and inefficient to fabricate them on the bottom of the substrate.

2.3.2 *pn* junction diodes

Unlike the Schottky diodes *pn* junction devices, including *p-i-n* and Avalanche photodiodes (APD), are more feasible as far as fabrication compatibility is concerned. Although it is difficult to imprint any complicated pattern directly on the sidewall, it still should be possible to define broad regions within the cavity via photolithography. In fact one extreme case would be to dope the entire inner wall, and figure 2.5 shows a 3-dimensional design and a bottom view of such device. The silicon nitride cantilever is included in the figure, in which the *n*+ region can be doped via diffusion. The bottom view shows the wiring of the *n*+ region and *p*+ contact of the *p*-type substrate. Moreover by choosing an appropriate resistivity/carrier concentration of the substrate, this device can be viewed either as *pn* junction diode or as PIN diode.

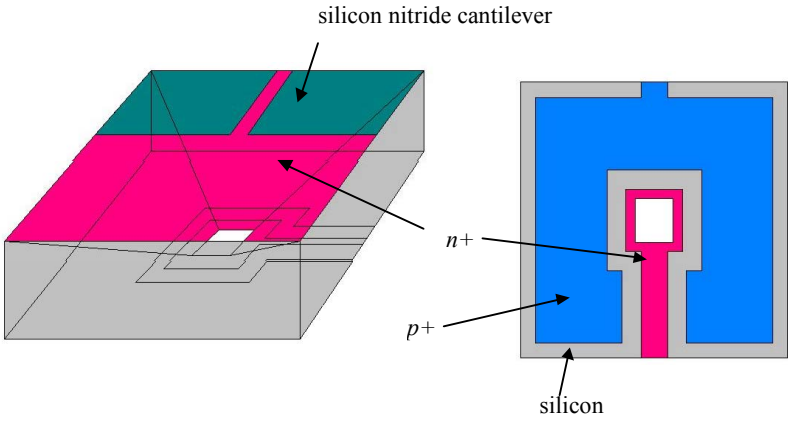

Figure 2.5: 3-D design and the bottom view of *pn* junction cavity.

If such a device is placed under high reverse bias, in simplistic views, the diode would be in breakdown region referred as avalanche breakdown. As photons generate EHP within depletion region extra EHPs are created by impact ionization originated from the single EHP. The actual breakdown voltage would depend on the doping concentration, but they are in the range of 10V~1000V for N_d of 10^{17}~$10^{14} cm^{-3}$ in the

case of abrupt *p+/n* junction [2.13, 2.14]. Nominally APDs have better amplification/sensitivity compared to *pn* junction diodes because of this internal carrier multiplication; however, since the sensor is to be operated under aqueous environment, APD may not be a good choice as it requires high voltage power supply for biasing. Not only that requiring such a high power source for a portable device is also less appealing. Additionally dark current in APD are larger than that of *pn* junction diodes because of the internal gain, and this may results in smaller signal-to-noise ratio. Similar argument is presented in an article with numerical examples based on commercially available photodiodes [2.15]. (Sensitivity = 30 A/W for APD and 0.6 A/W for *pn* diode; but dark current = 1nA and 100fA, respectively)

For the above reason, APD is also excluded, and this leaves *pn* junction and PIN diodes. Similar argument about too highly resistive substrate with extremely long diffusion length limiting distance between cavities for multi-analyte detection, presented in the previous section, is applicable to PIN diode as well; a EHP generated by photon may find its way into neighboring electrode if the diffusion length is very long. Therefore the design in this project is mainly based on *pn* junction diode for the above reasons and for its simplicity which also translates into lower cost. In general depletion width created at a *pn* junction is quite thin, and low quantum efficiency results from it. Although PIN has better efficiency due to the artificial insertion of the thicker intrinsic/depletion region, the abrupt *n+-p* junction built on a commonly available silicon wafer, grown by CZ (Czochralski) method with moderate doping concentration of N_A=$10^{15}cm^{-3}$, should be sufficient enough. It can be numerically shown that depletion width of *n+/p* junction with $N_D \sim 10^{20}cm^{-3}$ and $N_A \sim 10^{15}cm^{-3}$ with moderate reverse bias of about -5V is about $3\mu m$, which should be thick enough to absorb most of photons with wavelength of 400~500*nm* within the depletion region.

2.4 PAST WORK

2.4.1 Dielectric cantilevers for confining microspheres

After introducing the basic platform, efforts have been made to upgrade the original structure. One of the efforts is the addition of overhanging cantilever layers to confine the beads within their designated cavities during introduction of fluid samples. Figure 2.6 shows a SEM (Scanning Electron Microscope) picture of single layer cantilever made out of $Si_3N_4/SiO_2/Si_3N_4$ dielectric stack.

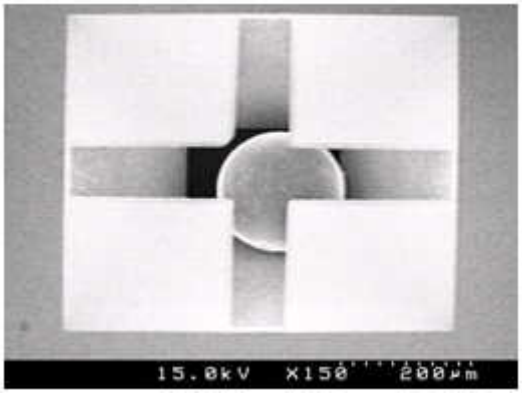

Figure 2.6: SEM picture of single layer cantilevers [2.16].

One of the constraints for any type of modification for the sensor array, including the proposed integration of photodiodes, is that the chemically derivatized bead has to be placed within the cavity after the fabrication in order not to disturb/alter the chemical properties. For the above device the bead is pulled down to the cavity while the cantilevers are deflected by placing a vacuum source underneath the bottom opening. Figure 2.7 shows two SEM pictures of bi-layer cantilevers.

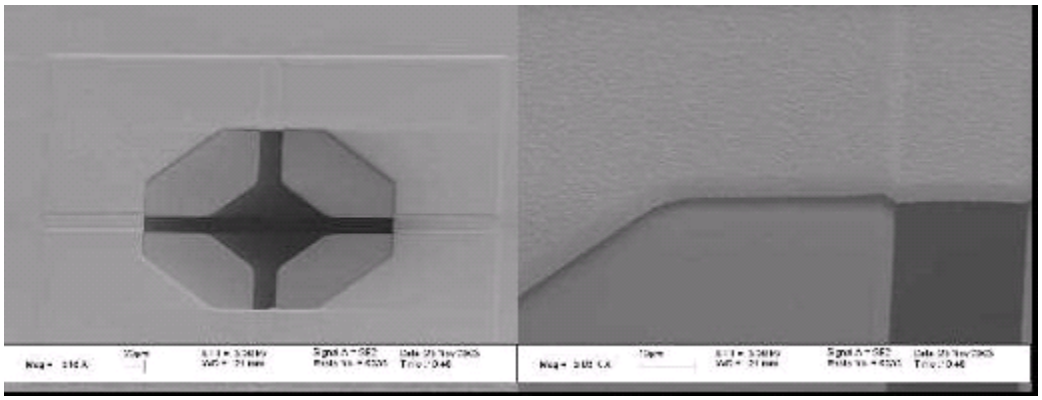

Figure 2.7: SEM pictures of bi-layer cantilevers [2.16].

The electron discharging is visible on the left picture because the lower cantilever and the upper cover layer are physically isolated, and the outer parameter which is the base of the pyramidal cavity is visible. Just like the single layer device a bead can be pulled down through the cantilever. The physical functionality of the chip is to restrict upward movement of the lower cantilevers, and by placing an additional cover layer on top of the entire structure, the effective opening can be controlled which would reduce diffusive leakage from one cavity to another. Both the upper and lower layers are silicon nitride (flow rate of DCS: NH_3 ~ 4: 1), and the sacrificial layer between the two layers are poly-silicon. Once all three layers are stacked and patterned, the entire structure is released monolithically with single KOH etching. If possible these types of confining cantilevers are to be integrated along with the photo-detector.

2.4.2 Anti-Reflection coating via single layer of silicon nitride

Another work that has been done relative to the project is the anti-reflective coating on the cavity. In the past to enhance the imaging of the fluorescence detection, anti-reflection coating to reduce the reflection on the sidewall of the cavity was investigated. Reduced reflection translates into increased absorption. Figure 2.8 shows a diagram of mediums considered for calculating the reflectivity, and how the physical layers interpreted as transmission line.

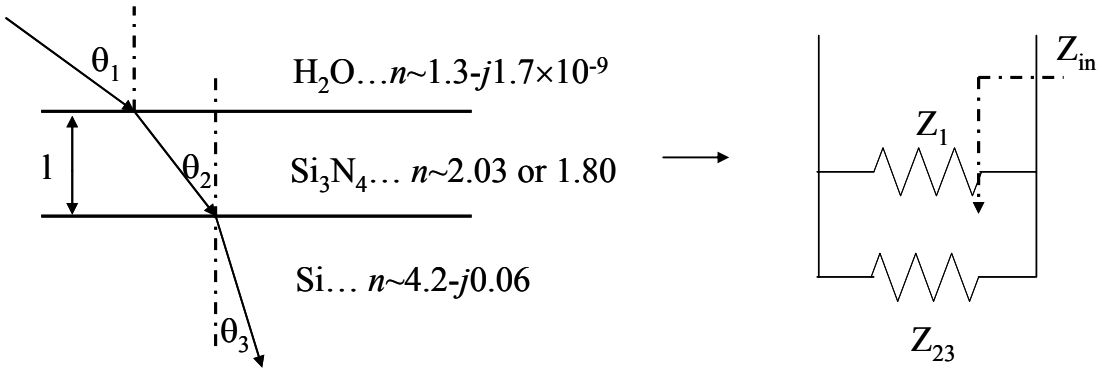

Figure 2.8: Diagram light transmitting through water, silicon nitride, and silicon substrate, and how they are analogized into transmission line.

In figure 2.8 wave impedance representing each layers are $Z_i = (\mu/\varepsilon)^{1/2} \times \cos(\theta_i)$ for TM mode, and $Z_i = (\mu/\varepsilon)^{1/2} \times \sec(\theta_i)$ for TE mode. Once the impedance are calculated, the combined impedance of silicon nitride layer and silicon, Z_{23}, can be calculated using

$$Z_{23} = Z_2 \frac{Z_3 + Z_2 \cdot \tanh(\gamma_2 l)}{Z_2 + Z_3 \cdot \tanh(\gamma_2 l)} \quad (2.1)$$

where l is the thickness of silicon nitride layer, and γ_2 is the propagation constant through the nitride layer, which can be found by $\gamma_i = j2\pi/(\lambda/n_i) \times \cos(\theta_i)$ for TM mode and $\gamma_i =$

$j2\pi/(\lambda/n_i) \times \sec(\theta_i)$ for TE mode. Once the characteristic impedance is calculated the overall input impedance is simply $Z_{in} = Z_1 || Z_{23}$. And the reflectivity, Γ, can be found by the Fresnel formulae, $\Gamma = (Z_{in} - Z_1)/(Z_{in} + Z_1)$. The graph in figure 2.9 is plotted using these formulae. However because the light detected from a sphere is practically a radiant source, meaning the angle of incidence, θ_1, at the sidewall is not normal and varies, the thickness of the AR layer is optimized based on an incident angle of 55° (Figure 2.9), which targets to minimize the light bouncing upwards toward microscope.

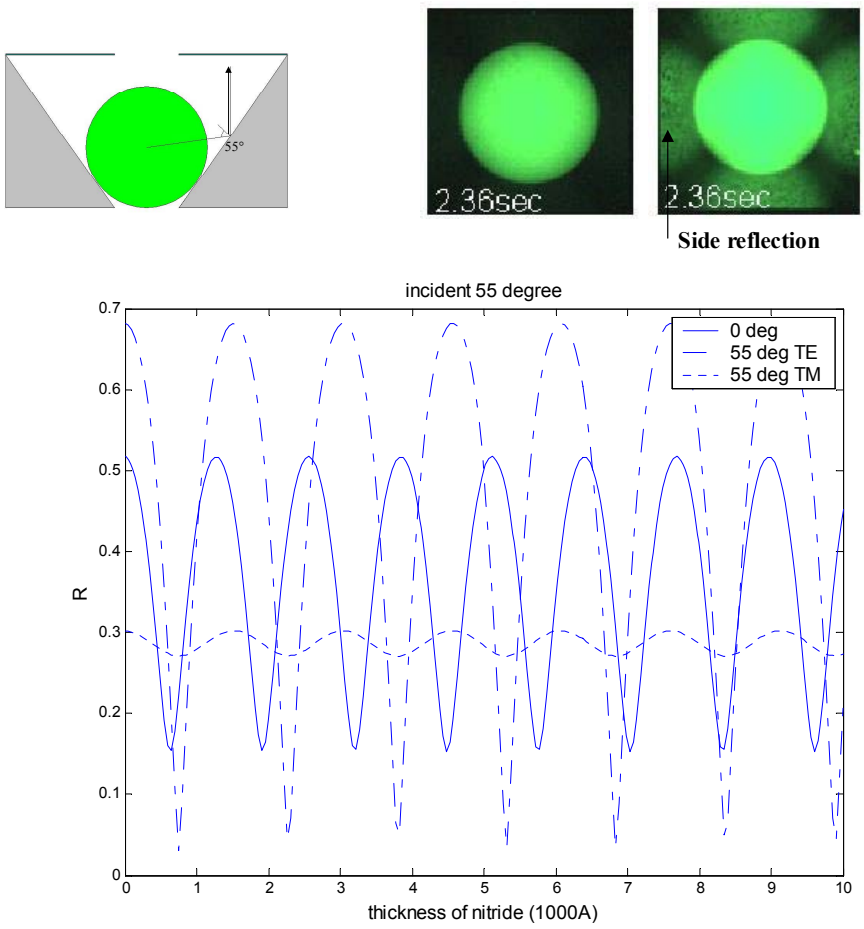

Figure 2.9: AR layer thickness calculated with Matlab along with 55° incident angle.

As it turns out 750$\mathring{A}$ thick silicon nitride layer is determined to provide minimum reflection at 520nm with the consideration of both TE and TM modes. Figure 2.8 also shows the pictorial result of the effort. The recorded intensity indicates that the reflection was reduced by (hence the absorption is increased by) up to ~50%. Additionally a similar strategy can be utilized to increase the reflectivity at the cantilever to contain as much photon as possible by introducing an intermediate layer such as metal (for broad band mirror) or poly-silicon (for wavelength dependent reflector).

2.5 *PN* JUNCTION PHOTODIODE BASICS

2.5.1 General parameters of a photodiode

The following list, extracted from chapter 2 of reference [2.1] and chapter 13 of reference [2.10], points out some of the requirement for a "good" chemiluminescent detector based on the four parameters that characterize the performance of a photodiode.

- Responsivity: the output signal of the detector should be directly related to the light intensity of the source.
- Spectral response: it should be sensitive over the wavelengths from 400nm to 600nm, at least. Preferably, the coverage be over the entire visible spectrum, 380nm~750nm.
- Detectivity: the detector must be able to detect light signal with various intensities.
- Time response: the response time should be faster than the chemiluminescent reaction rate.

Out of the four parameters the time response is the least critical factor for the proposed device. Unlike a photodetector used in optical communication, the photodiode is to detect single chemical reaction that occurs in the range of milliseconds; hence, the detector is optimized for other parameters when there is a performance tradeoff between time response and sensitivity. The following sections describe basic equations regarding

pn junction photodiode. The overall active area is assumed to be the entire sidewall of the pyramidal cavity. The device parameters are calculated by using conventional diode equations, and the differences, raised by fabricating the diode on a sloped wall, are pointed out when necessary.

2.5.2 Responsivity

Responsivity is defined as how much current is generated per unit radiated power, and it is directly related to the quantum efficiency. (R = $q\eta/hv$, where η = quantum efficiency) In a reverse biased *pn* junction photodiode, the photon enters the semiconductor and generates EHP within depletion region. The EHPs are swept away by electric field generated by built in voltage plus reverse bias, and they give rise to the drift current. Hence the efficiency is directly related to how much light enters the semiconductor (transmittivity or 1-reflectivity), how many of those photons reach the depletion region, and how many are absorbed within the depletion region. According to the reference [2.10], efficiency is defined as:

$$\eta = (1 - R^2) \cdot e^{-\alpha d} \cdot [1 - e^{-\alpha w}], \quad (2.2)$$

where R is the reflectivity, $e^{-\alpha d}$ represents the photon transmitted by the semiconductor with thickness of d before reaching the depletion region, α is the absorption coefficient, and w is depletion width where photons are absorbed. Any EHP generated within d are likely to be recombined and do not contribute to the current signal.

Anti-reflection coating of a single silicon nitride layer can significantly reduce the reflection coefficient between liquid and silicon. Figure 2.10 shows a similar graph of the reflection coefficient versus thickness of the AR coating by plotting the Fresnel formulae. Contrary to the previous graph, the interested incident angle is between 0~30°, emphasizing on the area where the bead sits tangentially to the sidewall and where the

light is vertically hitting the sidewall. The same index of refraction are used, for silicon = 4.196 - j0.056, for silicon nitride = 2.03, and for water = 1.33659 + j1.74×10^{-9}. [2.17, 2.18] Additionally the absorption coefficient for silicon is 1.2×$10^{4}$$cm^{-1}$ at the wavelength of 500nm [2.19]. Each plot represents reflectivity with different incident angle, and they are average of TE and TM mode. One thing to note is that they have periodicity, and the lowest reflections at different incident angles converge at the first minima. By depositing a single layer of silicon nitride with a thickness of ~620$\mathring{A}$, the reflection coefficient is expected to drop to about 30% on average.

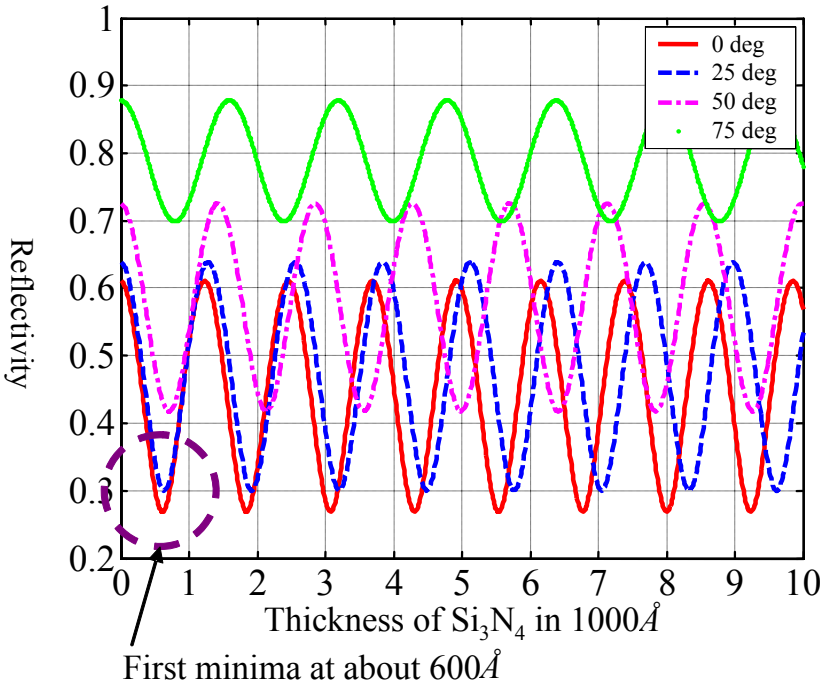

Figure 2.10: Reflection coefficient of water, Si_3N_4, and Si interface optimized at an incident angle of 0~30° with wavelength = 500nm.

The remaining parameters depend on the physical design of the *pn* junction and the doping concentration of *p/n* region. In order to increase η one of the doped regions, *d*, needs to be as thin as possible so that less photons are absorbed while traveling through the region before reaching the depleted area. Additionally the depletion region needs to be as thick as possible to increase *w*. It is no secret that *pn* junction with asymmetrical doping concentration are commonly used to increase the depletion width. Therefore the strategy is to fabricate *p+/n* or *n+/p* junction with minimal thickness on the heavily doped side. Looking at the equation for η, the absorption rate for silicon is reduced exponentially as the depth increases. Using the $e^{-\alpha d}$ term, the heavily doped region should be in the order of $100\mathring{A}$ to transmit 99% of the photon that enters the active area. Although EHP created within one diffusion length to the depletion region has a chance to diffuse in and contribute to the current signal, this aspect is less significant since highly doped semiconductor is expected to have very high recombination rate/shorter diffusion length due to shorter lifetime. On the other extreme for the depletion region to absorb 99% of the photon that enters the region, referring to $[1-e^{-\alpha w}]$ term, the depletion width needs to be about $3.84\mu m$. Figure 2.11 summarizes this section as an illustration.

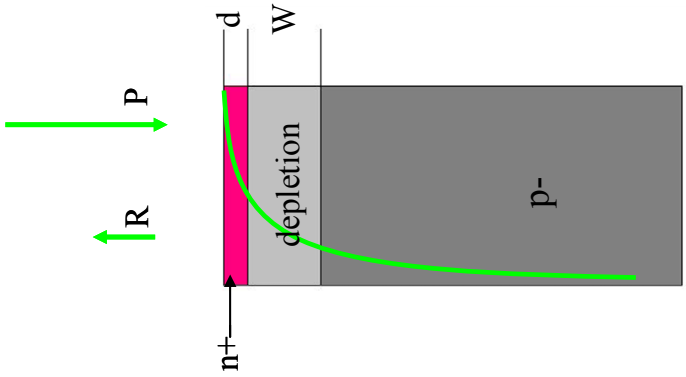

Figure 2.11: summary of photon absorption for an *n+/p* photodiode.

2.5.3 Detectivity (Dark Current)

As defined earlier detectivity indicates the lowest signal power that the photodetector can detect, and this is usually quantified as noise equivalent power (NEP), which is signal to noise (S/N) ratio equaling one. The dark current of a diode determines the noise in a photodetector, i.e. diode current without any light signal. The first component of the dark current is the saturation current of the photodiode. By forming a *pn* junction built-in potential develops at the junction due to minority carrier diffusion. By applying a reverse bias this field and depletion region is widened, there is carrier extraction occurring at the edge of the depletion region, and this drift current is the main source of the saturation current. The equation for the saturation current density given in reference [2.14] is

$$J_0 = q(\frac{D_p}{L_p} p_n + \frac{D_n}{L_n} n_p), \text{ (2.3)}$$

where D is the diffusivity of minority carrier, L is the diffusion length of the minority carrier. p_n refers to hole concentration in *n* region, and n_p refers to electron concentration in *p* region. The D and L can be obtained by

$$D = \frac{kT}{q}\mu, \text{ and } \quad L = \sqrt{D\tau}, \text{ (2.4 and 2.5)}$$

where μ is the mobility and τ is the minority carrier lifetime. Therefore the saturation current is determined by concentration, mobility, and lifetime of minority carriers. For the case of one-side heavily doped junction characteristic of lighter doped region dominates. In addition to the saturation current, generation current is another source of the dark current. While the saturation current is drift current of minority carriers swept away from the boundary of the depletion region, thermally generated EHP within the

depletion region also participate in the drift. In reference [2.13] the generation current density is given by

$$J_{g-r} = \frac{qn_i W}{\tau}, \quad (2.6)$$

where W is the depletion width and τ is the generation lifetime. Hence, "the total reverse current can be approximately given by the sum of diffusion components in the neutral region and the generation current in the depletion region" [2.20]. For semiconductors with low intrinsic carrier concentration, such as silicon, the generation current dominates [2.20]. Figure 2.12 is also acquired from the reference [2.20], which is referenced from [2.21], and it shows the current voltage characteristic and ratio of an ideal silicon diode and a practical diode.

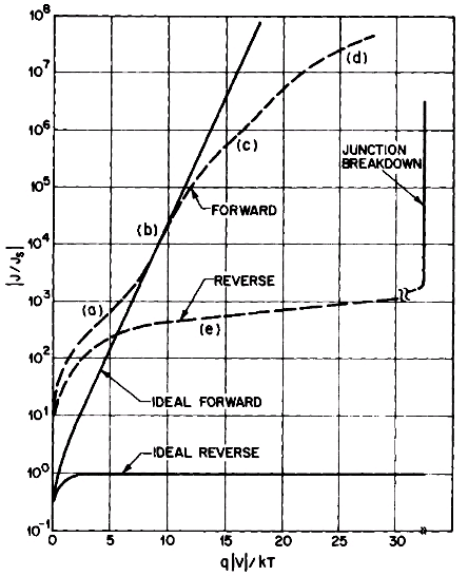

Figure 2.12: Ideal and practical current voltage characteristics of forward biased and reverse biased p-n junction [2.20, 2.21].

Other sources of dark currents are surface leakage current and tunneling current [2.22]. Tunneling current does not affect silicon as much because this phenomenon is mainly associated with direct band-gap materials operating at higher bias voltage. The surface leakage strongly depends on the fabrication process as it is proportional to the surface defect density, and it would be difficult to predict the surface leakage current. For the time being, the analysis is based on the ratio of $J/J_0 \sim 10^3$ at $q|V|/kt = 30$ provided by the figure 2.11. As an example, for a *p+/n* junction with $n_0 \sim 10^{15}$, $\tau_h = 12\mu s$, and $\mu_p = 400 cm^2/Vs$. Then $D_h \sim 10 cm^2/s$ and $L_h \sim 1.1\times10^{-2} cm$, resulting in $J_0 = 3.29\times10^{-11} A/cm^2$ and $J_{g\text{-}r} = 1.2\times10^{-7} A/cm^2$. As expected $J_{g\text{-}r}$ term dominates, and $J_{g\text{-}r}/J_0$ is about 3.5×10^3.

Once the dark current is calculated noise can be estimated as well using standard equations available for photodiodes used in optical communication, and detailed discussions on the noise can be found in references [2.10, 2.22, and 2.23]. Normally for detecting signals in optical communication systems, there is effective bandwidth associated with sampling time. However in practical sense sampling time is negligible in this application as the detector is monitoring a continuous signal for threshold type detection unless a chopper/pulse is applied to liquid source. Therefore DC dark current is used as the starting point of detectivity throughout.

2.5.4 *n+/p* junction versus *p+/n* junction

In general *p+/n* junction photodiodes are preferred over *n+/p* junction photodiodes because it has faster response time, i.e. $\mu_e > \mu_h$ therefore it takes less time for electrons generated within depletion region closer to the surface to reach the bulk (toward *n*), and due to longer minority carrier lifetime, i.e. $\tau_h > \tau_e$ when bulk doping concentration of *n*-type substrate and *p*-type substrate is the same, *p+/n* junction exhibits lower saturation current as well, which results in lower dark current. On the other hand *n+/p* photodiodes are preferred for detecting light with shorter wavelength close to UV, and such an

example of UV-enhanced silicon photodiode can be found in reference [2.24]. The reasoning behind this is partially explained in section 2.5.2: more photons are absorbed closer to the surface, i.e. the transmittance drops exponentially. Additionally the absorption coefficient, α, is inversely proportional to wavelength; hence, light with shorter wavelength is absorbed near the surface at much faster rate. Therefore the first doped layer that light hits, *d* in figure 2.10, needs to be as thin as possible especially for light with shorter wavelength, and potentially *n*+ region can be fabricated thinner than *p*+ region because *n*-type dopants exhibit less diffusivity. This phenomenon coincides with the fact that solubility limit of boron (B), a typical *p*- type dopant, is lower than that of arsenic (As) or phosphorus (P), meaning that higher *n*-type concentration can be achieved at lower temperatures, and lower temperature means shallower junction. All the mentioned fabrication-related characteristics are well described in the literature such as reference [2.25]. And reference [2.26] and [2.27] shows ion implantation profile of shallow junctions.

Roughly speaking the ratio of junction depth fabricated with As diffusion and B diffusion is about 10^{-4} estimated by the ratio of diffusivity with same diffusion time but different temperatures to obtain similar surface concentration. (T = 900°C for As and T = 1100°C for B) In order to place that number into perspective, assuming the target junction depth equal to $100\mathring{A}$ for As, which will transmit 99% of photons with $\lambda = 500nm$, the depth of junction made with B targeting similar concentration will be about $100\mu m$, absorbing all the photons in *p*+ region at the same wavelength. Although calculation in the above is rather an extreme scenario, it does illustrate that *n+/p* junction is more suitable for detecting lights close to UV region.

Chapter 3: Preliminary experiment on passive RFID tag

3.1 EAS TAG CIRCUIT BASICS

3.1.1 Ideal case of simple RC tag circuit

This section describes basic circuit theory relevant to the passive EAS-tag like wireless system. Figure 3.1 shows a) the circuit diagram consisting of a reader coil, tag coil with a capacitive load and b) the equivalent circuit found by replacing the magnetically coupled coils into T-equivalent circuit [3.8]. In reality both coils and the load would have associated resistive element, but this simpler example is chosen to illustrate the circuit behavior with much simpler numerical equation.

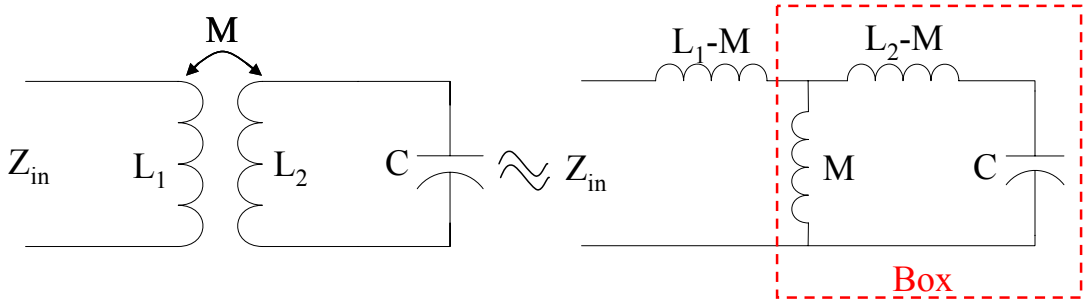

Figure 3.1: simple tag circuit with inductive coupling and equivalent circuit.

An example of this type of sensor can be found in reference [2.2]. The reference points out that the phase plot of input impedance behaves like magnitude plot of a transfer function of a band reject filter, and vice versa the magnitude behaves like the phase. Center frequency of the "phase dip" is used to analyze the state of the transducer, and these topics are addressed here. First the admittance on the right, around the load in red-dashed box, is

$$Y_{box} = \frac{1}{j\omega M} + \frac{1}{[j\omega(L_2 - M) + 1/j\omega C]} = \frac{j[\omega(L_2 - M) - 1/\omega C] + j\omega M}{j\omega M \cdot j[\omega(L_2 - M) - 1/\omega C]} \quad (3.1)$$

At this point please note that the $j\omega M$ terms in the numerator are going to cancel each other out. Hence the input impedance of the system is

$$Z_{in} = jw(L_1 - M) + Z_{box} = jw(L_1 - M) + \frac{jwM \cdot j[w(L_2 - M) - 1/wC]}{j(wL_2 - 1/wC)}$$

$$= j\frac{w(L_1 - M)(wL_2 - 1/wC) - wM[w(L_2 - M) - 1/wC]}{(wL_2 - 1/wC)} \quad (3.2)$$

The phase of Z_{in} is $\tan^{-1}$ of the above term, and it reveals why there is a phase dip and where the phase dip occurs. The denominator in the above equation represents the imaginary part of the tag impedance, and the resonance of such RLC circuit occurs at inverse geometrical mean of L and C, where the imaginary part becomes zero. Although it is not apparent in the above equation, both numerator and denominator are negative vales; hence the phase of the input impedance stays near +90° away from the resonant frequency. However at the resonant frequency, the phase suddenly approaches -90°, which is $\tan^{-1}(-\infty)$, as the denominator becomes zero. As an example, the above equation is plotted using Matlab, and figure 3.2 shows both magnitude and phase plot of the above circuit with ideal values of $L_1=4\mu H$, $L_2=4\mu H$, $M=1\mu H$, and $C=200pF$. The resonant frequency of this tag is $(1/2\pi) \times (4\cdot10^{-6}\times200\cdot10^{-12})^{-1/2} = 5.63\times10^{6}$Hz, where the phase dip occurs close to that frequency.

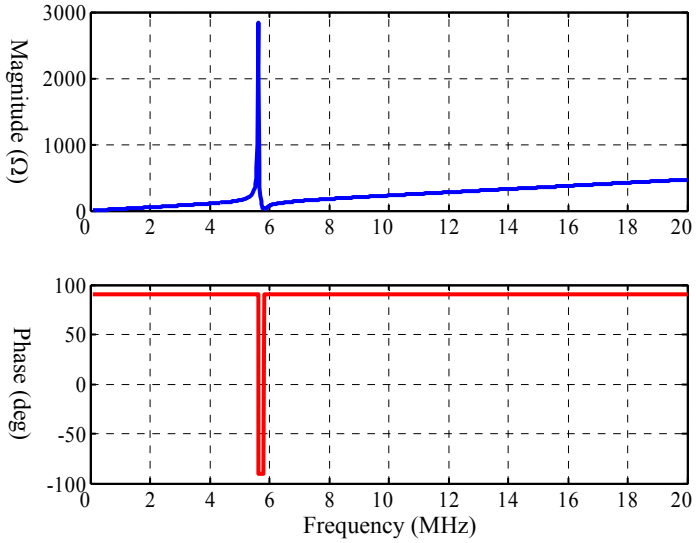

Figure 3.2: Ideal magnitude and phase response of input impedance when reader coil is magnetically couple with LC tag circuit.

3.1.2 Ideal case with resistive elements

Previous analysis of ideal LC tag circuit is carried out even further by placing resistors next to both coils as shown in figure 3.3 a), where R1 represents the resistance of the reader coil and R2 represents the resistance of the transmitter coil and wires that connects the coil and capacitor, and b) the magnitude and phase response of input impedance. (R1 = 1Ω, R2 = 10Ω, and rest are the same)

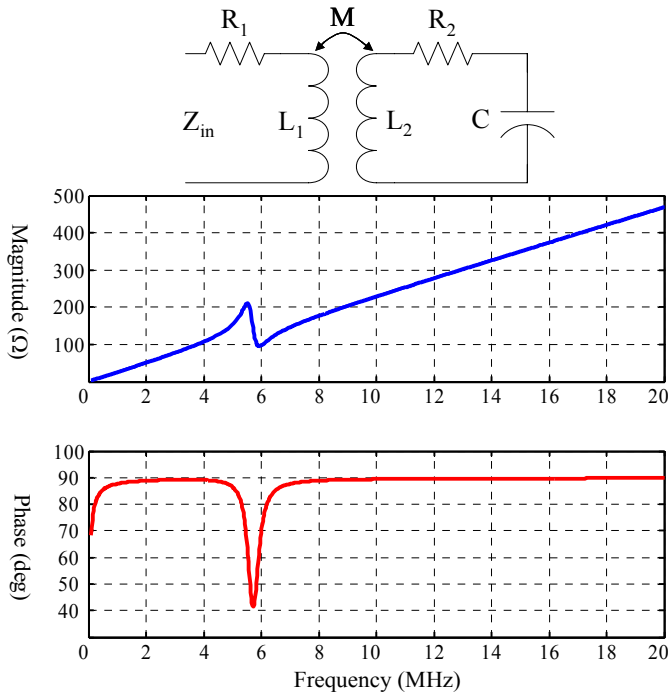

Figure 3.3: Magnitude and phase response after inclusion of resistors.

The shape of each graph has changed by the placement of small resistors, and they are more representative of a measured response. Figure 3.4 shows two phase plots of a) different R1 and b) R2. All the other values remained the same. Although the dips in b) appears to be broader, the solid red line when R2 = 10 is identical to all the other cases. The effect of R1 and R2 is very clear. Larger R1 hinders the phase response reaching 90° as frequency increases, and if the resonance is too close to it, the phase dip may be effected as shown when R1 = 20Ω. The actual phases are 41.4°, 39.1°, and 36.7° as R1 increases. Larger R2 produces shallower phase dip, and the width of the dip becomes broader. The actual phases at resonance were 6.1°, 41.4°, and 64.3° as R2 increased. As predicted, all six responses show resonant frequency of 5.72~5.73MHz.

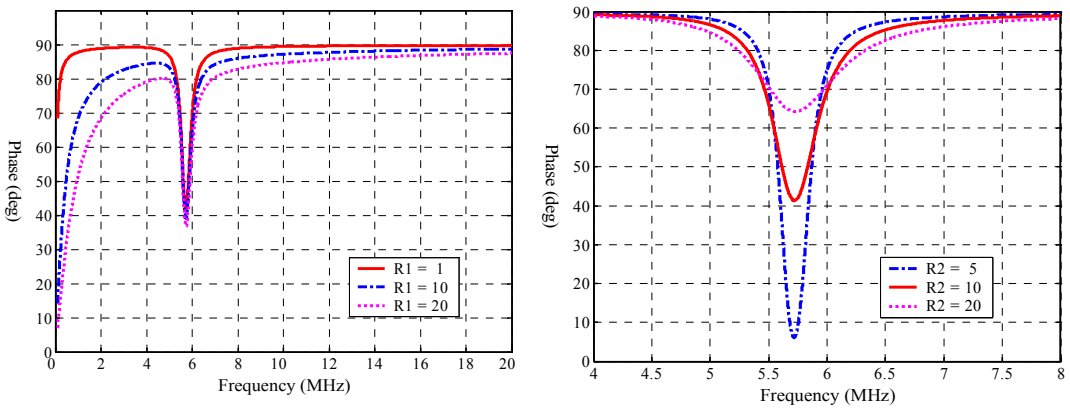

Figure 3.4: Phase plot of the input impedance with varying a) R1 and b) R2.

3.1.3 Effect of the coupling efficiency

Another element that affects the input impedance is the mutual inductance, *M*. As indicated earlier, *M* can be expressed in terms of coupling efficiency, *k*. Figure 3.5 shows phase plots with varying *k*, a) from 1% to 10% and b) from 10% to 100%. Intuitively when *k* is 100%, referring to the equivalent circuit, the response completely changes to that of a parallel LC circuit.

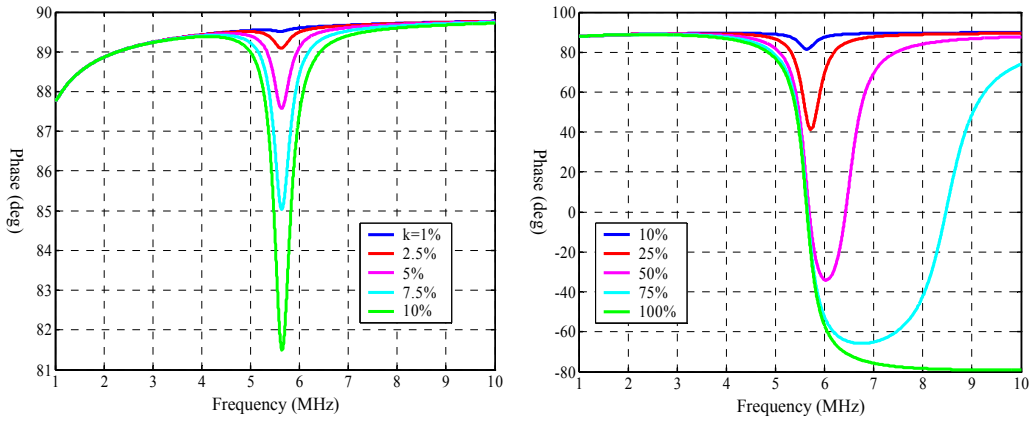

Figure 3.5: phase response with varying coupling factor.

As shown in figure 3.5 center frequency where minima of the phase dip occur is affected by change in the coupling efficiency. The center frequency departs further from the tag resonant frequency as the coupling efficiency increases. When k is 100%, no matter how unrealistic this is, the phase response is significantly different. As it turns out, the phase is pulled down close toward -90°, and it bounces back up and saturates to 0° at about 2GHz. Although this type of extremely high coupling efficiency is unlikely to be obtained in real life, the overall trend of deviating center frequency with increasing coupling efficiency is troublesome. Therefore this phenomena is analyzed further by plotting k vs. $(\omega_{c(k)} - \omega_{c,\,tag}) / \omega_{c,\,tag}$ and k vs. the actual phase at the minima, as shown in figure 3.6.

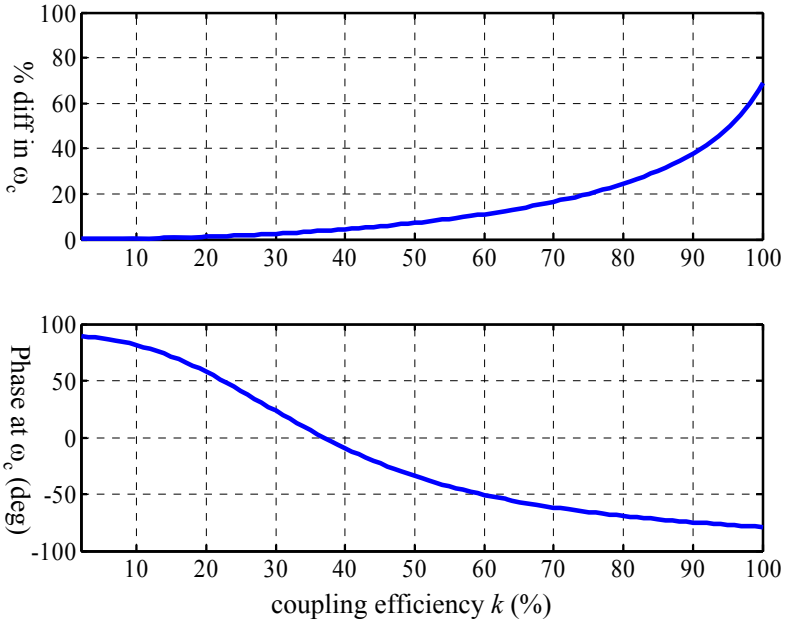

Figure 3.6: Effects of coupling efficiency on center frequency.

In the above figure, normalized difference between center frequency of the phase dip and the tag resonant frequency reaches 10% when k = 57.5%. The effect of coupling factor is also pointed out in reference [2.2], and it reveals that the effect is influenced by R_2 as well. The overall effect is negligible when k is low, which is shown here as well. However unlike the sensors used in reference [2.2], it is likely that much higher k can be achieved as the overall circumstance of measurement is different. Although it is a bit early to make any conclusions at this time, the effect of coupling efficiency will be kept track of as it certainly influences the location of the phase dip.

3.1.4 Effect of the capacitive load

The effect of the capacitive load is also considered. When the capacitance increases, the resonant frequency of the tag should be changed, and different phase dip is anticipated. Figure 3.7 shows phase plots of different capacitive loads.

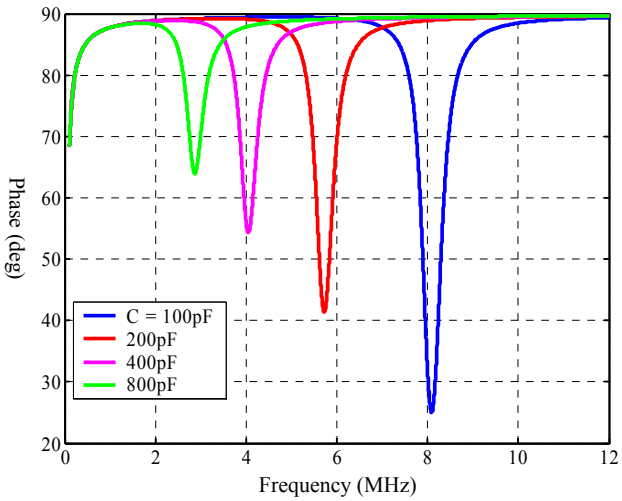

Figure 3.7: phase plot of different capacitive loads.

As expected, for large capacitance, the phase dip occurs at lower frequencies. It should be noted that the magnitude of the phase dip is also reduced. In all four occurrences, the dips are located very close to the tag resonant frequencies. On a side note, the width of the phase dip decreases as the capacitance increase; although the width of 800pF dip is slightly larger than that of 400pF dip, the reason for this is because the dip is also affected by the roll up at low frequency.

3.1.5 Effect of the inductors

Effects of the inductors are also considered as well. As the physical parameter of the coils dictates the inductance, the coupling efficiency would be affected as the inductance varies, but in this calculation, the coupling efficiency was set to be constant. For this analysis, $L_2 = m \times L1$, where m varies from 25% to 400%, and this is plotted in figure 3.8.

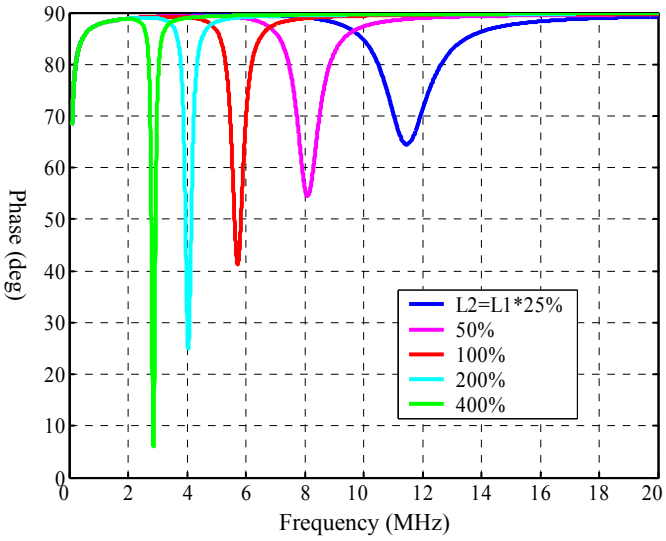

Figure 3.8: effects of inductors on the phase response.

Again, as L_2 increases, the tag resonant frequency decrease, and the phase dip occurs at lower frequencies. As shown in the figure 3.7 the amplitude of the phase dip becomes larger, and the width becomes narrower. For all practical purposes, when L_1 varies while L_2 is constant, the phase dip does not change although smaller L_1 has similar effect as larger R_1; hence, larger L_1 has sharper corners.

3.1.6 Summary of EAS tag circuit

Effects of different circuit elements on the phase response of EAS tag circuit are reviewed. Although only a capacitive load is considered here, effect of real, positive imaginary, and negative imaginary impedance of an equivalent tag circuit of different loads should be similar. What has not been discussed is that the ultimate sensitivity is influenced by the variance in capacitance/load as it is the sensor. Once the capacitance is known, other elements can be chosen for sharper response signal. One aspect to keep track of is the effect of coupling efficiency, as it alters the center frequency.

3.2 PRELIMINARY EXPERIMENT WITH COMMERCIAL PHOTODIODE

Commercially available silicon PIN (*p-intrinsic-n*) photodiodes, S6967, are purchased from Hamamatsu [3.1] to test and demonstrate the feasibility of wireless detection of chemiluminescent reaction. The idea is to monitor the change in resonant frequency of the photodiode, which is induced by a chemiluminescent reaction. The photodiode is connected to an inductor, i.e. a loop of wire, and this inductor is magnetically coupled to another inductor, i.e. a reader coil. The change in resonant frequency is recognized by observing the change in the input impedance of the reader coil with a gain-phase analyzer, Hewlett-Packard 4194A. Hence, unlike conventional DC (Direct Current) measurement of photodiodes, the light is detected via non-contact AC (Alternating Current) measurement. Additionally DC experiments with a commercially

available photodiode would be a good benchmark in comparison with photodiodes fabricated at this institution.

3.2.1 Hamamatsu S6967

In general the small signal model of a diode for high frequency response consists of a parallel combination of the small signal resistor, r_d, the depletion layer junction capacitance, C_j, and the diffusion capacitance, C_d [3.2]. It is expected that the DC current response of a photodiode would be very sensitive to photons, and the change in the DC current would result in the change in AC resistance. Addition to this, in order to maximize the AC response for this initial wireless demonstration, a photodiode with large capacitance was sought after, although this usually meant a photodiode with large active area. The effective active area of Hamamatsu S6967 is 26.4mm^2, the dark current at -10V bias is 500pA, the terminal capacitance at -0.1V is 200pF, and the responsivity for 500nm light is 0.3A/W; all values are quoted from the specification sheet.

3.2.2 Experimental setup

Figure 3.9 shows the experimental setup for the demonstration. A BNC coaxial cable is used to connect the reader coil to HP 4149A. The transmitting coil is placed in the proximity of the reader coil, and it is connected to a light shielding black box with another BNC coaxial cable. Inside of the box, the photodiode is simply hooked up to the BNC terminal with a mini grabber clips. Hp 4149A is controlled with a desktop computer with National Instrument's LabView software.

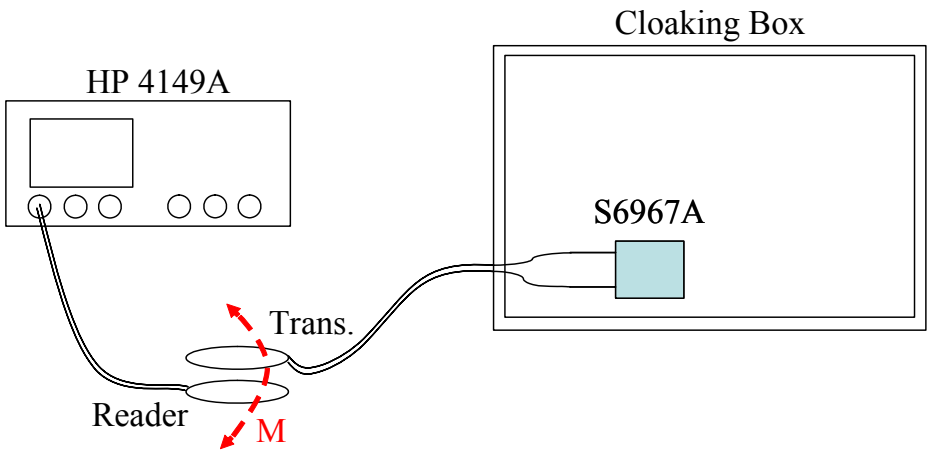

Figure 3.9: Diagram of the experimental setup.

It is important to note that the above setup contains a lot of parasitic elements. Between the transmitting inductor to the photodiode, the coaxial cable still has finite parasitic capacitance and the mini grabber contributes to additional inductance and resistance. Therefore the information read by the reader coil would include the effects of these parasitic elements as well.

3.2.3 Modification to S6967A

In an effort to roughly quantify the volume of chemiluminescent specimen, four cylindrical cavities with 1mm diameter are drilled on a 1mm thick plastic sheet, and this plastic plate is attached onto the photodiode. The volume of each cylinder is about 1.7μL. Figure 3.10 shows the picture of modified and standard S6967 silicon PIN photodiode. As shown in the figure, a capacitor with the value of 470pF is soldered onto the positive terminal, i.e. positive bias voltage on this terminal would put the diode in forward bias, and this device is to be connected to a hand-wound coil with an inductance of about 3.5uH.

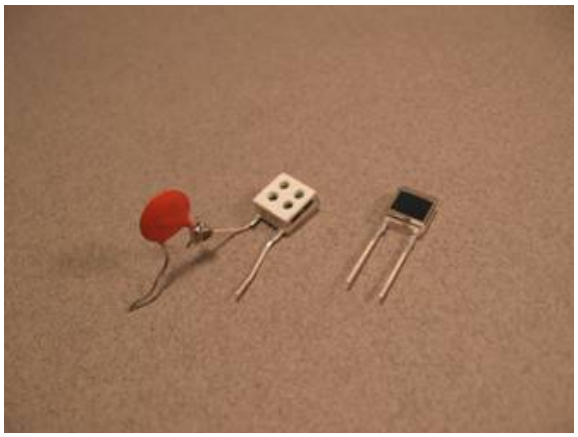

Figure 3.10: photography of S6967A with plastic cavities along with non-modified S6967A.

3.2.4 Light stick as the light source

As the actual chemistry to be used with the detector was still under the development, a known and stable chemiluminescent reaction is used to test the structure for verifying the idea. The green colored chemiluminescent sample was extracted from a commercially available light stick manufactured by UNIQUE IND., INC. This type of sample provides very bright light for a long period of time up to several hours, which makes a sound source for the experiment.

A lot of information is available on-line regarding these light sticks, widely used from military applications to everyday entertainment purposes. Typically it is made out of a plastic tube containing phenyl oxalate ester and a fluorescent dye, and this compound is isolated from hydrogen peroxide contained in a glass vile inside of the plastic tube [3.3]. The light stick is bent to be activated, which breaks the glass vile and mixes the hydrogen peroxide with the chemical compound, and these results in chemiluminescence.

3.3 EXPERIMENTAL RESULTS AND DISSCUSION

After performing a search to ensure that the chemicals contained in these light sticks are reasonably safe, they are cut at each end of the plastic tubing after activating them to extract the content to an open container. A syringe is used to transfer the extracted compound to the photodiode described in section 3.2, and each cavity is filled with the compound one at a time.

3.3.1 Magnitude and phase of Z_{in}

Figure 3.11 shows the graph of the input impedance of the reader coil measured with HP 4149A as each cavity is filled. The graph on the left is the magnitude plot and on the right is the phase plot.

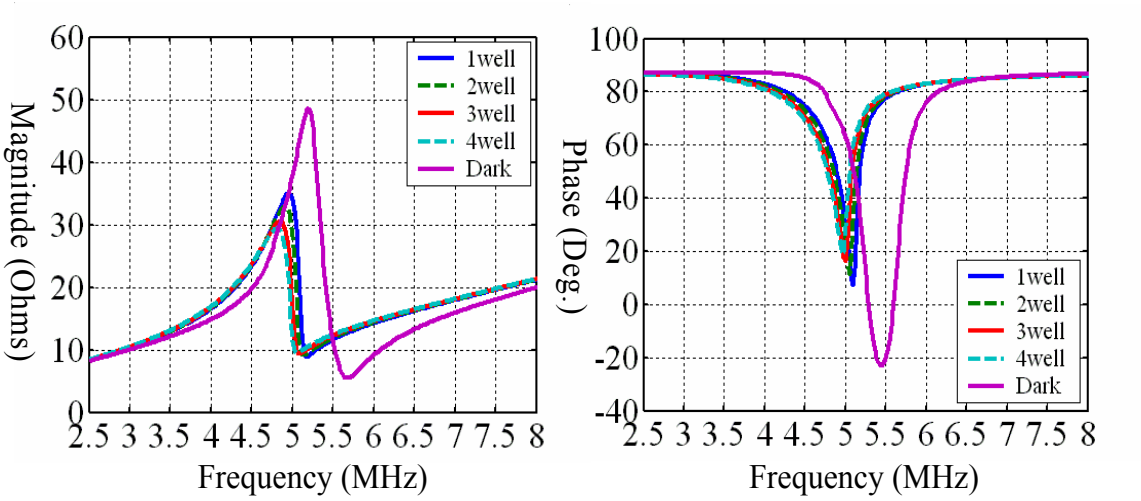

Figure 3.11: Magnitude and phase plot of the input impedance measured by HP 4149A.

The phase plot on the right shows the "phase dip," and the resonant frequency is indicated by the lowest point of the dip. It is evident even with these graphs plotted from the raw data that there is a clear difference between "dark/off" state and "light/on" state. In fact just a few percent changes in the resonant frequency would be detectable. Although it may appear that the actual change in the magnitude or the phase would also

be useful, it is not as indicative because those changes depend on how well the inductors are coupled, which will vary from each measurement; whereas, the center frequency would not [3.4].

3.3.2 Measured data

Table 3.1 shows measured values from the graphs in figure 3.3: specifically the resonant frequency ω_0 and the maxima and the minima of the magnitude plot ω_1 and ω_2. Additionally, pseudo-Q, reminiscent of the quality factor in a magnitude plot of a transfer function, is presented. Pseudo-Q (pQ)is defined as

$$pQ = \frac{\omega_0}{\Delta\omega} \qquad (3.3)$$

where $\Delta\omega$ is 3dB-down width, "defined as the full-width half-max (FWHM) of the phase curve." [3.4] A few tens of percent changes in pseudo-Q would be detectable. During the AC measurements, DC measurements are carried out simultaneously, measuring the diode current with reverse bias of 5V with HP4140, a pico-amp meter.

	Dark	**1 well**	**2 wells**	**3 wells**	**4 wells**
ω_0 (MHz)	**5.455**	**5.095**	**5.050**	**5.005**	**4.960**
pQ	**7.82**	**25.9**	**28.7**	**33.9**	**37.4**
I (nA)	**0.439**	**45.0**	**100**	**136**	**182**
ω_1 (MHz)	**5.21**	**4.96**	**4.92**	**4.85**	**4.83**
ω_2 (MHz)	**5.68**	**5.16**	**5.14**	**5.1**	**5.07**

Table 3.1: Measured resonant frequency, converted pseudo-Q, measured reverse biased current, maxima and minima of magnitude plot of S6967 photodiode detecting chemiluminescent light, extracted from light stick.

3.3.3 Discussion

The dark current of 0.439nA at -5V is in a good agreement with the specification, and although it is ambiguous to define a signal-to-noise ratio for the DC current measurement because the light source is considered to be uniform, a hundred fold increases from the dark current should not present any problem. In fact a constant increase of the reverse biased current, on the average of 45nA, indicates that there is a constant increase in the number of photons absorbed by the photodiode, which reassures that the four cavities are geometrically similar. Figure 3.12a shows the percent change in ω_0, ω_1, ω_2, and average of ω_2 and ω_1 to the respective values at dark state as a function of number of cavities filled with chemiluminescent sample, and the data points are fitted using Matlab. Figure 3.12b shows comparative plot of $\Delta\omega$, the FWHM, and ω_2-ω_1 from the magnitude plot.

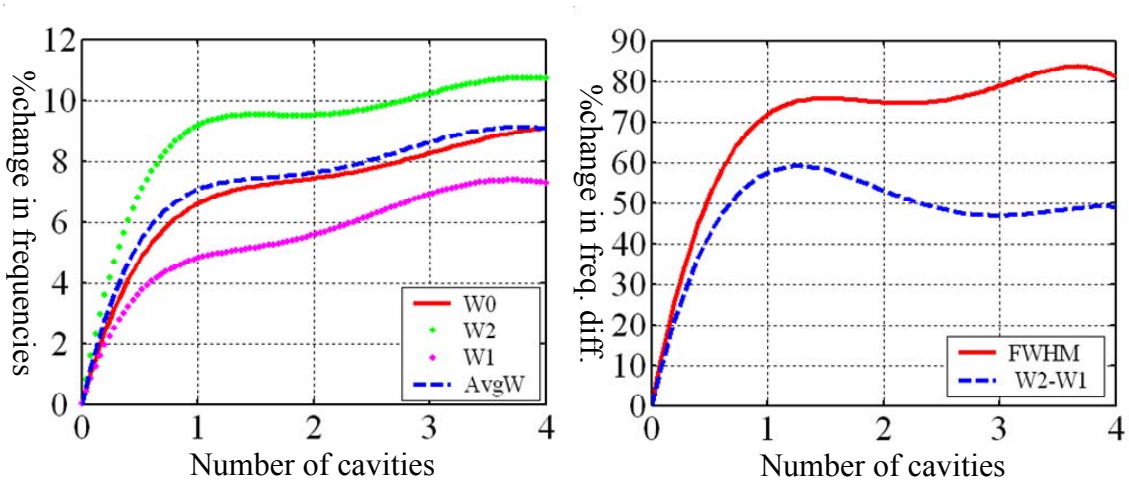

Figure 3.12 fitted plots of a) percent change in ω0, ω1, ω2, and average of ω2 and ω1 and b) percent change of Δω, the FWHM, and ω2-ω1 from the magnitude plot.

Observing that the changes in the difference of the ω_2 and ω_1 from magnitude plot, as shown in figure 3.12b, decrease as cavities are filled suggest that it is not a good variable to keep track of compared to $\Delta\omega$. Figure 3.13 shows the plot of percent changes in pseudo-Q (pQ_0) and alternate pseudo-Q's, obtained by replacing ω_0 in equation 3.3 with ω_2 (pQ_2) and ω_1 (pQ_1).

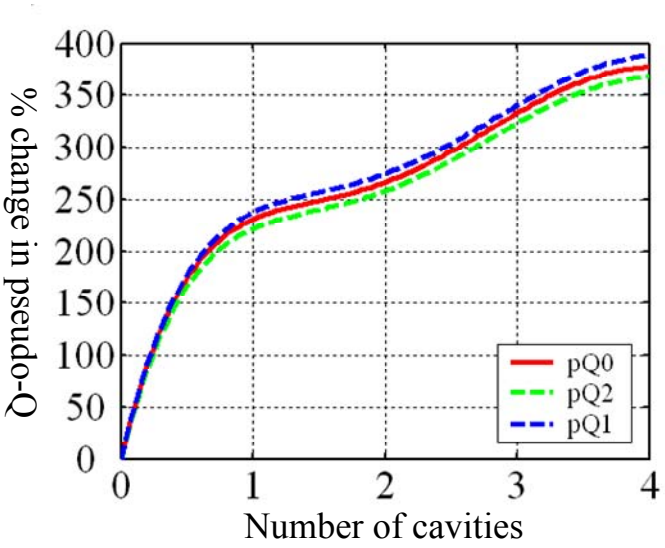

Figure 3.13: percent changes in different pseudo-Q's.

It is encouraging that over 200% change in pseudo-Q is observed in this preliminary experiment. Although the change in pseudo-Q1 appears to be slightly greater than the change in pseudo-Q0, figure 3.13 confirms the fact that ω_2 and ω_1 of the magnitude plot is closely related to ω_0.

3.4 ANALYSIS OF THE SILICON PHOTODIODE

Earlier in section 3.2.1 it is pointed out that the small signal model of a *pn* junction diode is a parallel combination of a resistor and capacitors; however, the small signal model of a PIN diode is different. Although there are elaborate RF models of a

PIN diode, such as presented in reference [3.5], more traditional model in reverse biased condition consist of an inductor, a capacitor and a resistor connected in series [3.6].

In order to gain better understanding of the AC behavior of the photodiode modulated by a light source, the commercial silicon PIN photodiode was directly measured using the gain-phase analyzer. HP 41491A impedance probe, which includes a standard calibration kit, was used to extend the port to the cloaking box and make the measurement. With the measured data, efforts are made to extract the values of the inductor, capacitor, and resistor. First, the imaginary part of the measured data were used to match L and C using $Z_{Im}=j\omega L+1/j\omega C$. Although it's difficult to distinguish them, figure 3.14 shows two plots of the measured and calculated Z_{Im} when the photodiode was in dark.

Matlab was used to perform this task. Initially, a starting values of C and L was determined based on the manufacturer's data sheet, in this case C = 150pF and L = 0.1μH. Then, these values are swept from 1 to 1000% of their starting value through the Z_{Im} equation, and the code was written to determine the set of L and C that provided minimum sum of the difference in absolute values of the two throughout the measure frequency. Once L and C are determined, resonant frequency, where the imaginary term would be close to 0, is determined and R is read off from the magnitude response at the frequency. Figure 3.15 shows the magnitude and phase plot of the measured Z_{in} of the commercial photodiode in dark and that of the calculated R, L, and C in series. Figure 3.16 shows similar graphs when the photodiode is modulated with light stick compound.

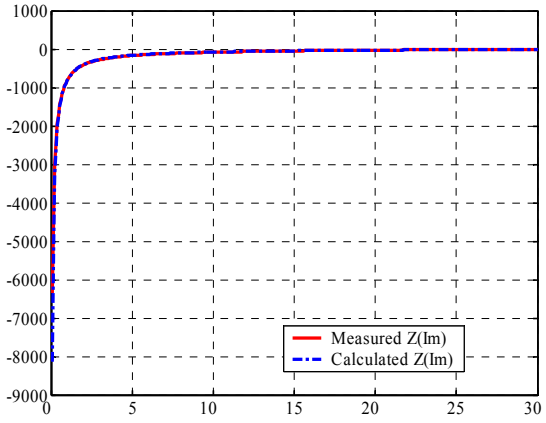

Figure 3.14: Plots of the measured Z(Im) of the commercial SIN photodiode and calculated Z(Im) using the extracted L and C.

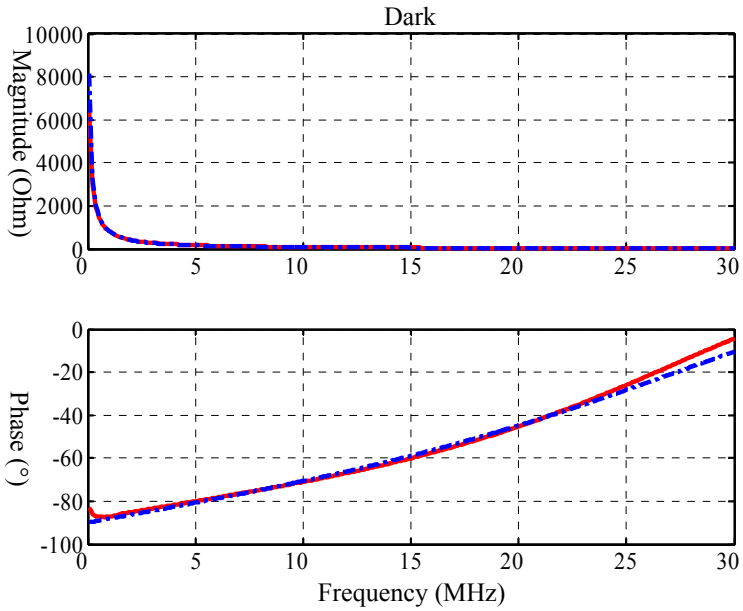

Figure 3.15 Magnitude and phase plots of the measured input impedance and calculated impedance using extracted R, L, and C in series.

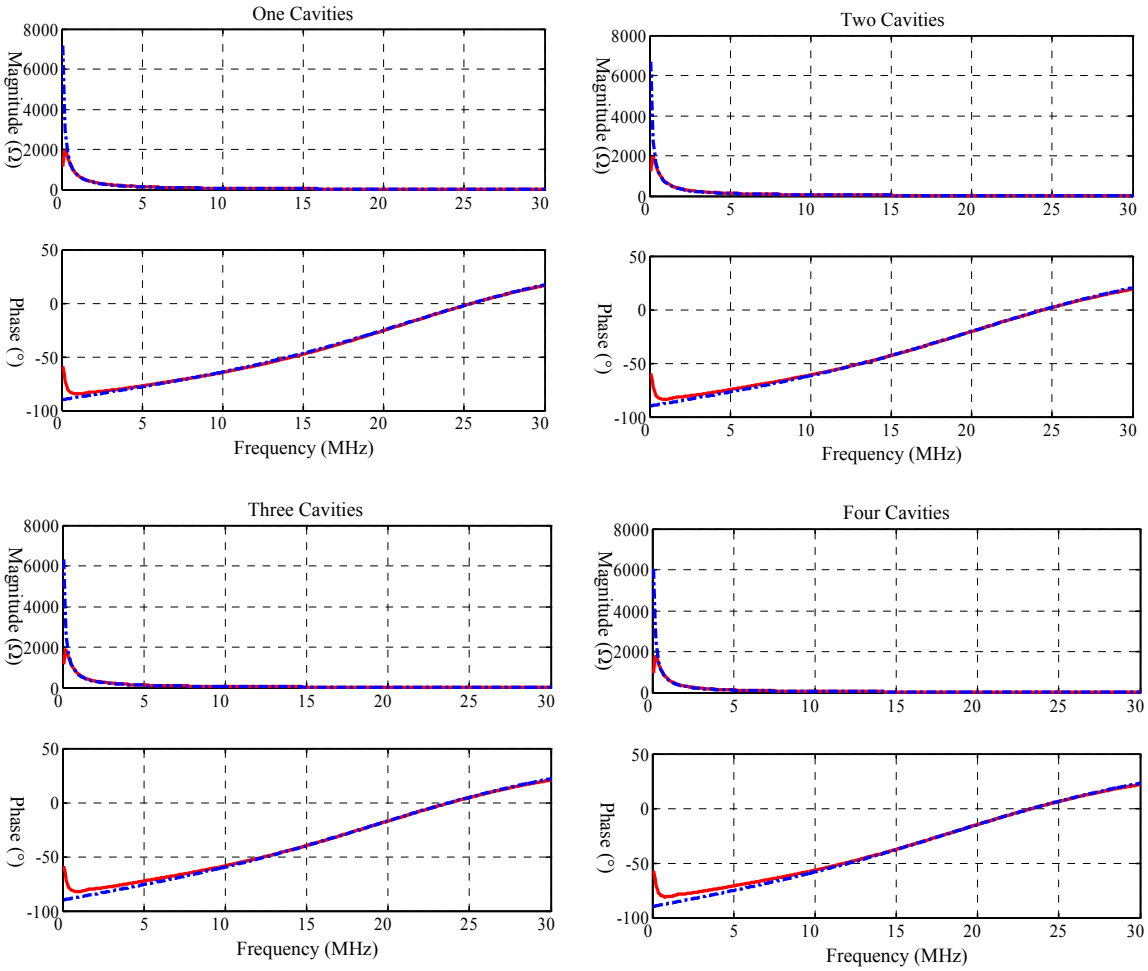

Figure 3.16: Magnitude and phase plots of the measured input impedance and calculated impedance using extracted R, L, and C in series of silicon PIN photodiode modulated by chemiluminescent light stick. Each cavity is ~785nL.

Once the RLC values are determined for the photodiode in dark, those values are used as the starting point for finding the change in the RLC values when the photodiode is modulated approximately by 1.7μL of chemiluminescent light stick compound at a time with the same Matlab code. Table 3.2 shows the extracted RLC values for various states.

	R(Ω)	L (nH)	C(pF)
Dark	**26.5**	**118**	**196**
One cavity	**29.6**	**176**	**211**
Two cavities	**30.1**	**177**	**238**
Three cavities	**30.5**	**177**	**252**
Four cavities	**30.7**	**176**	**263**

Table 3.2: Extracted RLC values from the measured impedance.

First of all the small signal model of silicon PIN diode, RLC in series, is a very reasonable model as it matches the measured data at the wide range of frequency. Looking at the figure 3.8 as the photodiode is illuminated with more and more photons, i.e. more cavities are filled, the overall magnitude drops. Additionally observing the phase plots the photodiode is initially dominated by the capacitance, but as the number of photons increases, the phase plots become more positive at higher frequencies. Both phenomena can be explained by the increase in the capacitance. Although there are minor increases in both resistance and inductance, overall characteristic is mostly affected by the change in capacitance as the impedance of a capacitor is $1/j\omega C$. Comparing the dark value and the values when all four cavities are filled, the resistance increases about 16%, the inductance increases about 49%, and the capacitance increases about 34%. Although the percent changes for inductance is greater than capacitance, positive phase is more likely the result of effect of capacitance being reduced at higher frequency as the magnitude of 1/C is much grater than L.

3.5 OVERALL ANALYSIS

After calculating the RLC values for the commercial silicon photodiode, they are used to run full circuit analysis using the EAS tag circuit model presented earlier. The capacitive load used in section 3.1.1 is now replaced with RLC in series. Figure 3.17 a) shows the circuit diagram and b) shows the measured phase response in dark and calculated phase response of silicon PIN photodiode in dark and when four cavities are filled. Both L_1 and L_2 are set to be $3.5\mu H$; however, it is difficult to know the exact coupling efficiency for the system. As the photodiode itself has moderate resistance, it should be the bulk of R_2. Therefore, it is likely that the only variable that the magnitude of phase response depends on, in this case at least in the dark state, should be k. For generating figure 3.9, $k = 0.5$ is used.

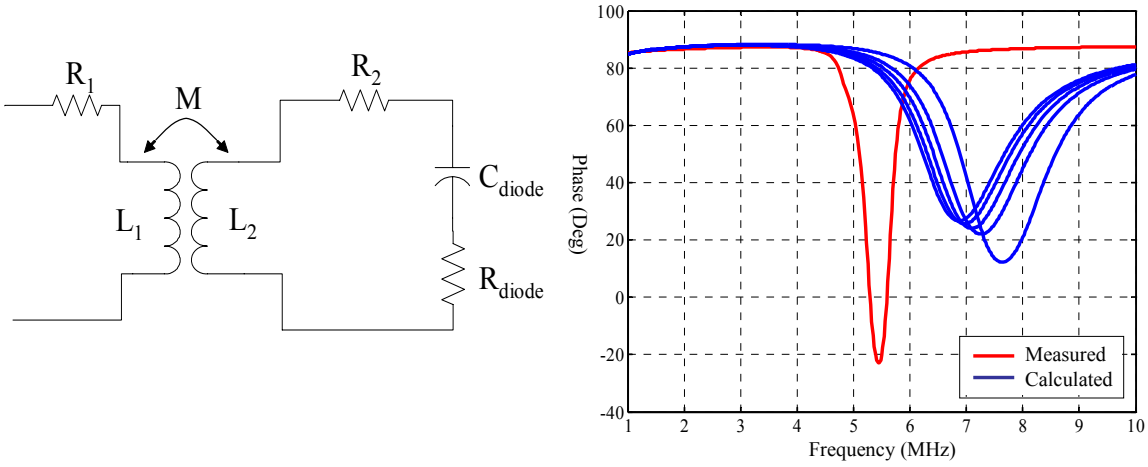

Figure 3.17: circuit model for EAS tag with silicon PIN diode as a load

Unfortunately, the phase response with calculated impedance did not match that of the measured data. As the initial demonstration was done over two years ago, it is difficult to duplicate the exact setting. And as pointed out earlier, the initial

demonstration was very hastily done, and it is highly likely that there were many parasitic elements present during the measurement. One in particular, the mini grabber that was used for connecting the photodiode and BNC cable could be a source of significant inductance because it forms a loop as it is connected to the phododiode. Efforts are made to at least match the responses in dark state by adjusting impedance with consideration of parasitic elements. Figure 3.18 shows graphs with measured phase response and calculated response. The circuit was adjusted by placing a parasitic inductance of 3uH in series, and resistance of the photodiode was reduced by 16.5Ω. The coupling efficiency is chosen to be k = 0.5. Two sets of graphs included in the figures are phase response in dark and with four filled cavities.

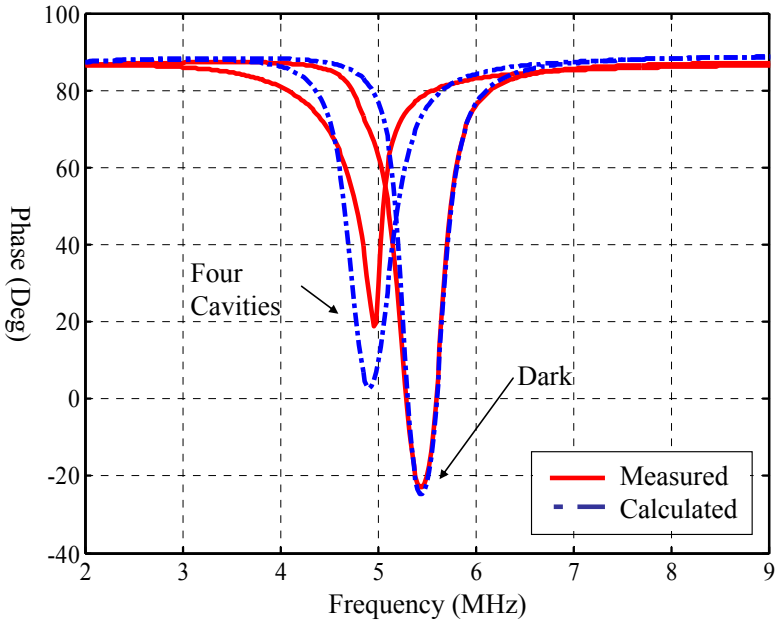

Figure 3.18: Comparison between measured and calculated phase dip.

There can be many explanations why the measured and calculated phase responses do not match, although the overall trend is there. The corners of the phase dip are asymmetrical for both measured and calculated responses, which indicate that k is

pretty strong. The center frequencies of the phase dips are reasonably close. Because AC measurements are very sensitive, if the amount of chemiluminescence compound that modulated the photodiode is different, the phase response would change. If the photodiode has moved ever so slightly while the sample is being loaded, for example, the response would have changed because both the parasitic inductance and coupling efficiency would have changed. There is no immediate explanation comes to mind why smaller R_2 resulted in better match, although a small parasitic resistance in parallel to the photodiode would have reduced the overall tag resistance significantly.

Additional efforts can be made to simulate the phase response and match the curves even further; however, for the time being, the analysis on the preliminary experiment is stopped at this point because the photodiode that is going to be used eventually will be *pn* junction diode rather than PIN. The overall analysis is valid as all the trends are there, and the knowledge gained from the preliminary experiment is carried over when designing the actual device. It is surprising that stronger *k* does not necessarily indicate that pseudo-Q is going to be higher. If possible, the difference in center frequencies of each phase dip should be maximized to differentiate between each state, while maintaining sharper shape of phase dips for higher pseudo-Q.

Chapter 4: Fabrication

This chapter describes efforts on integration of *n*+/*p* junction photodiodes inside bulk silicon micro-machined pyramidal cavities. Initially two batches of photodiodes were fabricated based on initially designed fabrication sequence; however, devices on both sets exhibited extremely high dark currents. Afterwards the entire fabrication sequence have been revamped and resulted in devices with acceptable electrical characteristics. All these fabrication sequences as well as the obtained knowledge and reasoning behind the alteration are presented in this chapter.

4.1 FIRST BATCH

This section describes efforts on the first batch of integrated photodiode within pyramidal cavity created based on the initial design on paper.

4.1.1 Experimental setup

Figure 4.1 shows 3 dimensional design and the cross sectional diagram of the integrated photodiode along with electrical connection illustrating how it would be measured. Although the electronic taste chip normally has opened bottoms for outlet, the KOH etching is terminated prematurely for the most of fabricated devices in order to minimize the complications on subsequent photolithography steps as photoresist (PR) is spun onto the substrate held on a vacuum chuck. It is possible to use second substrate as a backing during photolithography, but this triples the lithography time as the device wafers has to be attached on the backing substrate using PR and removed later on. For the design *p*+ plate is electrically connected to the brass chuck with a vacuum, the *n*+ plate is probed from the top, and the cavity can be accessed from the top.

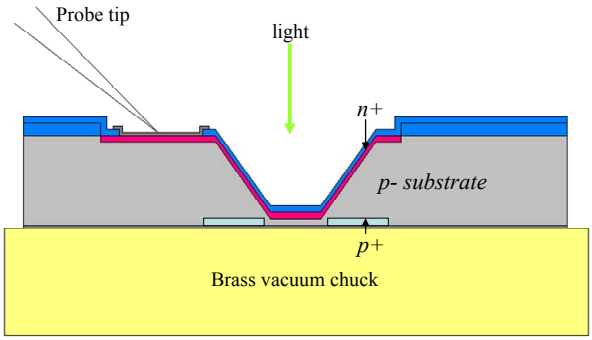

Figure 4.1: Experimental setup for p+/n+ contacts.

4.1.2 Fabrication sequence of the first batch

Figure 4.2 shows the fabrication steps of the design shown above. First a silicon nitride layer is deposited using PTL LPCVD on a 250μm thick *p*-type silicon substrate of ~25$\Omega \cdot cm$ resistivity. The gas mixture consists of dichlorosilane (DCS at 60sccm) and ammonia (NH_3 at 15sccm), the deposition temperature is about 835°C, and the deposition pressure is about 300mTorr. The thickness of the dielectric film is about 1500$\mathring{A}$, which is ample enough to be an effective masking layer for the subsequent ion implantation. [4.1] Next the square opening, which forms the base of the upside down pyramidal cavity, of about 450μm is patterned on photoresist (PR, AZ 5209, 40s at 4000rpm), and the square pattern is etched onto the silicon nitride layer using reactive ion etching (RIE, CF_4+O_2, 40mTorr, and 100watts). Afterwards the wafer is plunged into KOH to etch the pyramidal cavities at about 80°C for about 4 hours. For this first batch the KOH etching is terminated prematurely so that some silicon is left over at the bottom based on the reasoning described in the previous section.

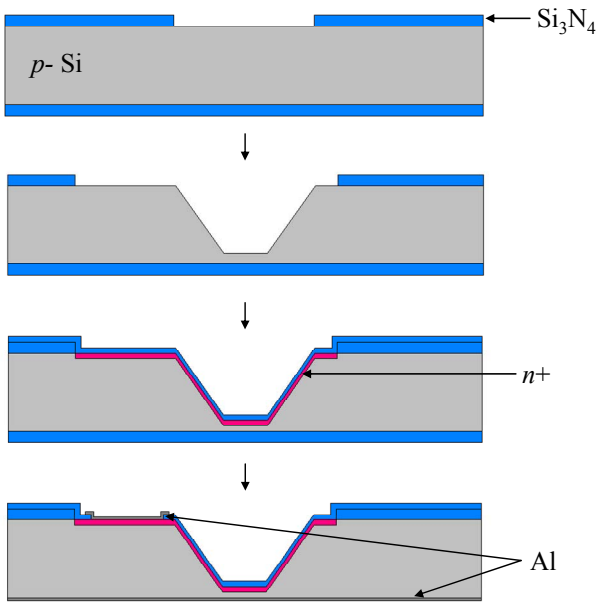

Figure 4.2: Fabrication sequence used on the first batch.

After the cavities are formed the wafers are cleaned with modified RCA2 cleaning, mixture of hydrochloric acid (HCL, 800ml), hydro peroxide (H_2O_2, 800ml), and DI water (H_2O, 800ml). This is followed by another application of PR on the top surface. Because the surface is no longer flat due to the cavities, PR is not applied evenly, which can be recognized by wave of colors surrounding the outer edges of the cavities. As it turns out, the PR around the cavities are lifted off during the soft contact photolithography. In order to get around this the PR is spin coated for longer duration of 60sec, and it is soft-baked for about 20min. Subsequently the rectangular window for the ion implantation is patterned and etched using RIE (CF_4+O_2, 40mTorr, and 100watts). The silicon substrates are then sent out for ion implantation at Nu Ions (San Jose, CA 95112). The *n*+ region is implanted with Arsenic (E=15keV, Q=1e15, 45° tilt, 7° offset).

After the ion implantation the wafers are cleaned with piranha cleaning (H_2O_2 800ml, H_2SO_4 1600ml, for 10 minutes) and modified RCA2 cleaning same as the above.

The wafers are then recoated with silicon nitride layer using LPCVD with the same recipe followed by rapid thermal annealing (RTA 1000°C for 30sec). The Si_3N_4 layer serves as protective layer and anti-reflection (AR) coating. And then smaller square opening for the contact was etched via photolithography and RIE. At the same time the silicon nitride on the back side is stripped using the RIE with the same recipe. The back side of the silicon substrate is then roughened using 200 grid sand papers; $p+$ layers were not used for the first batch. Aluminum is deposited using CHA evaporator (~2000$\mathring{A}$), patterned, and etched on the top side for $n+$ contact followed by blank Al deposition on the back side for the bulk substrate contact. Afterwards the device was sintered at 400°C for about 30 seconds.

4.1.3 Discussions and concerns

Initially all the current-voltage (I-V) measurement has indicated that there was a serious leakage current when the diode is in reverse bias. The dark currents were in 0.1mA range; however, because these are the first batch, it was difficult to pinpoint the cause of the problem. Using additional substrates in this first batch, in order to reduce surface leakage if there were any, the implanted wafer was plunged in hydrofluoric (HF) acid to strip Si_3N_4, and then the surface was recoated with SiO_2 deposited with LTO. It takes about 15 minutes to completely etch away ~1500$\mathring{A}$ thick Si_3N_4. Afterwards the contact opening is made, and Al is deposited and patterned. And then the wafer is cleaved in half, and only one half of the wafer is sintered. It is suspected that Kirkendall effect played a role on the huge dark current because the dark current is reduced down to about 0.5μA at -10V for devices that are not sintered. The breakdown, i.e. when $I_{dark} \sim 10\mu A$, has occurred at about - 30V. Because the $n+$ layer is quite thin, the Al contact must have

breached the junction and provided a leakage path to the bulk. For being a first batch the clear forward and reverse diode characteristic was encouraging; however, the dark current is just very large for this type of device. Additionally during the fabrication, some concerns have been raised. Figure 4.3 shows the IV curve of the photodiode fabricated within the pyramidal cavity.

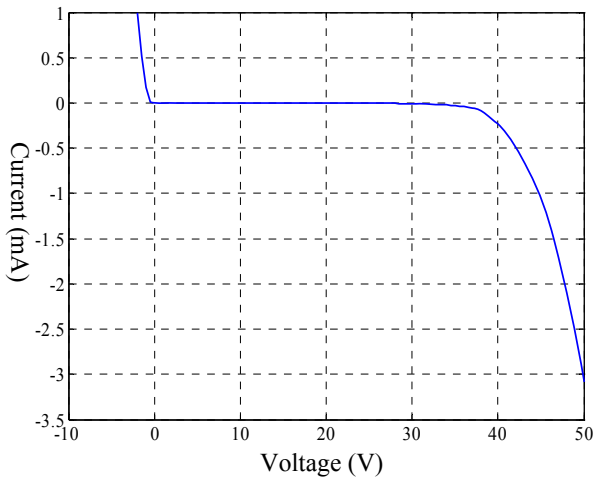

Figure 4.3: IV of photodiode fabricated in a cavity from the first batch.

The first concern is the Kirkendall effects. Implanting Arsenic at about 20keV is projected to have a junction depth of about 150*Å*. [4.1] In order to minimize the Kirkendall effects Al target containing silicon impurities can be used. The second concern is that because Si_3N_4 is used as the passivation layer, the implanted wafers were placed in 850°C furnace for about an hour. Although references state that the diffusion at such temperature is minimal, perhaps it would be better to use LTO, which deposits SiO_2 at about 530°C. This aspect will be investigated by fabricating two types with different passivation steps and comparing them for the second batch. Additionally following the KOH etching, RIE is used to etch the Si_3N_4 layer to define active junction area

surrounding the top opening, the second step in figure 4.2. Although the effect may be insignificant this step raises two concerns. First during the RIE etching the silicon pyramidal cavity is exposed and may be susceptible to plasma damage, which would create surface traps. Reduction of minority carrier lifetime during RIE can be found in literatures such as reference [4.21]. Second it is difficult to terminate the RIE at the exact interface of Si_3N_4 and silicon. Instead of using CF_4 and O_2, CHF_3 and O_2 can be used to etch Si_3N_4 and/or SiO_2, and it indeed has better selectivity against silicon although the etch rate drops to about 1/3. As silicon underneath the opening is etched definition of the boarder line between to be implanted *n*+ region and the bulk *p*- region becomes tricky. Figure 4.4 illustrates these points on a cross sectional view. In order to avoid possible plasma damage to the naked silicon surface as well as the over-etching of silicon, RIE will not be used to define the junction area; rather, wet etching will be used to etch either Si_3N_4 or SiO_2 masking layer.

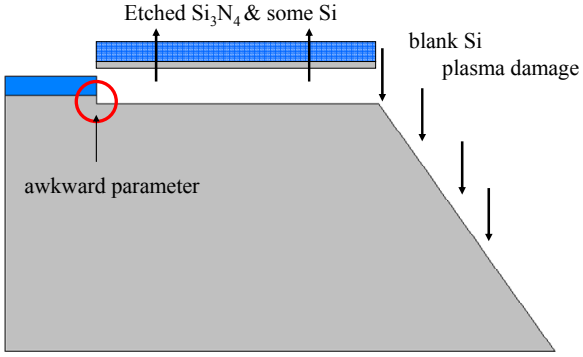

Figure 4.4: possible concerns during RIE after KOH etching. The blank silicon sidewall of the pyramidal cavity is exposed and susceptible to plasma damage on the silicon surface. Additionally the awkward step form by over etching of silicon at the boundary of to be implanted n+ region.

4.2 SECOND BATCH

After fabricating the first batch some of the possible problem areas were identified as discussed in the previous section. The second batch is fabricated to realize the design introduced earlier with an effort to eliminate those problematic areas, and the *p*+ bottom electrode plate is included.

4.2.1 Wet etching of Si_3N_4

As stated earlier one of the possible problems is using RIE (CF_4+O_2) to etch the Si_3N_4 layer as this may induce plasma damage to the silicon sidewalls on etched cavities and has poor selectivity against silicon. In order to avoid possible plasma damage on Si surface SiO_2 would be a better material as the masking layer for ion implantation because SiO_2 can be etched with buffered hydrofluoric acid (BHF), which has very good selectivity to silicon. However the problem with using SiO_2 layer is that the silicon dioxide layers are prone to KOH etching: this is the inherent dilemma. The dielectric layer is first used as a masking layer for KOH etching and then used as masking layer for ion implantation. Si_3N_4 is the preferred material for the KOH etching, and SiO_2 is the preferred material for masking ion implantation and as the passivation layer. The problem would be less complicated if Si_3N_4 can be wet etched; unfortunately, it is not easy to wet etch Si_3N_4. H_3PO_4 does etch Si_3N_4, but the etch rate is very slow (~100*Å*/min, [4.1]), not to mention that the solution needs to be boiled, which is not only cumbersome but also can be hazardous. First solution thought up for the problem was to initially deposit Si_3N_4 and use it as the masking layer for the KOH etching. Afterwards, the Si_3N_4 layer is striped using HF, and the substrates are recoated with SiO_2 And then, the active region would be patterned using BHF. Problem for this solution is that during the Si_3N_4 strip the bottom opening would be prematurely formed, and this complicates later fabrication steps

when substrate are to be held down by vacuum, i.e. spin coating PR, aligning/exposing, and etc.

In MEMS devices silicon rich silicon nitride is used as a structure material, which has lower mechanical stress compared to stoichiometric silicon nitride [4.2, 4.4]. As it turns out HF etching rate drops as the Si gas flow increases during the deposition of silicon nitride films. The gas flow rate of PTL LPCVD is modified to 44sccm of DCS and 5sccm of NH_3. For 49% HF acid, the etch rate for Si_3N_4 is about 100*Å*/min; where as, it takes about 60mins to etch 1000*Å* of SiN_x. (etch rate~17*Å*/min) For the second batch this selectivity is used to preserve the dielectric layer covering the bottom opening.

4.2.2 Fabrication sequence of the second batch

First SiO_2 layer is deposited using PTL LTO for a thickness of about 1500*Å*. One side is coated with PR, followed by a hard bake. The wafers are placed in BHF solution until SiO_2 on one side is completely etched away. After the PR is stripped, the wafers are loaded into PTL LPCVD for deposition of SiN_x. Now, the SiN_x, on top of the SiO_2 layer, is etched using RIE until SiO_2 is exposed. The wafers are placed back into BHF solution, and then, loaded into PTL LPCVD for deposition of Si_3N_4. Effectively the wafers are coated with Si_3N_4 on top and SiN_x on the bottom, and during the process, the silicon surface has not been exposed during RIE. Figure 4.5 shows the schematics of the process flow up to this point.

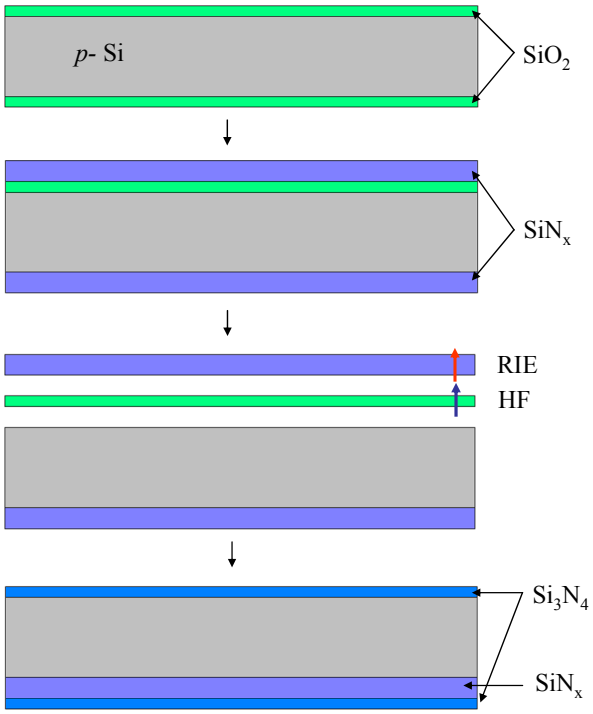

Figure 4.5: asymmetrical silicon nitride coating on wafers.

From this point, there are two variations to the fabrication flow. But first figure 4.6 shows the top view of the layout. The inner square is the base of the pyramidal cavity, which is surrounded by a larger rectangle. The entire rectangular area is to be implanted with arsenic, and the vacancy next to the cavity serves as the contact. Such geometry would result in larger dark current because of large contact area, but this layout is chosen considering the feasibility of fabrication and experimentation for demonstrating the concept of photodiode fabricated within a cavity.

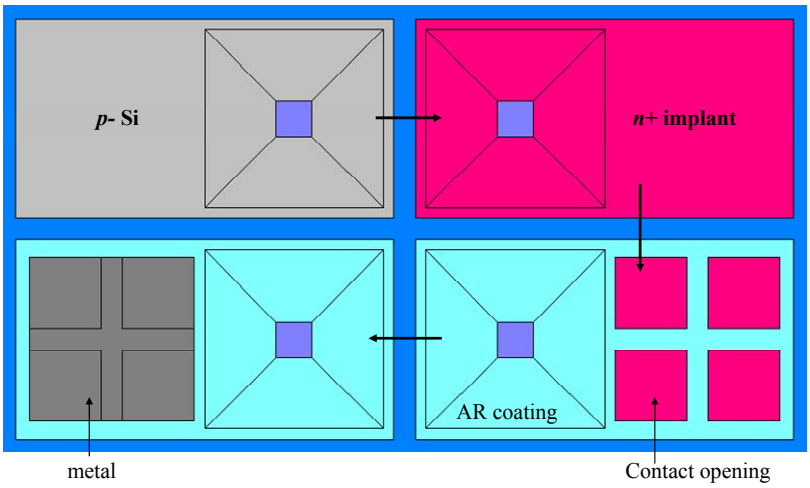

Figure 4.6: Layout of the device. This diagram actually shows the fabrication flow as well. Top left is exposed p-Si. Top right is after n+ implantation. Bottom right is after AR coating and opening of contacts. Finally, bottom left shows metal contact.

After the steps in figure 4.5 for type I, the square opening is etched via photolithography and RIE. The substrate is then etched with KOH, and the cavity is formed. Then, the entire substrate is plunged in HF acid until the top Si_3N_4 is etched away; during that time, only a fraction of the bottom SiN_x layer is etched. Once the top layer is completely removed SiO_2 is deposited with LTO, and the rectangle (top left drawing of figure 4.6) is patterned and etched with BHF. Overall for type I devices, SiO_2 is used as the masking layer for ion implantation, and later SiO_2 is used again as the AR coating.

For the second type devices a simpler sequence is used. First SiN_x is directly deposited, and then the rectangular opening is patterned with photolithography and etched with RIE (CF_4+O_2 followed by CHF_3+O_2). After removing the PR Si_3N_4 layer is deposited with LPCVD followed by patterning squares and KOH etching. After the

cavity is formed, the substrates are placed in HF until the top Si_3N_4 layer is completely etched, and SiNx layer act as the etch-stop. Compared to type I devices the fabrication step is considerably minimized; however, although the sidewalls are not directly exposed during RIE, the contact region was exposed. Gas combination of CHF_3+O_2 during RIE is used at the end because of its higher selectivity to Si; however, the awkward step mentioned in previous section may still exist. Figure 4.7 shows the fabrication sequence for both type I (on the left) and type II devices.

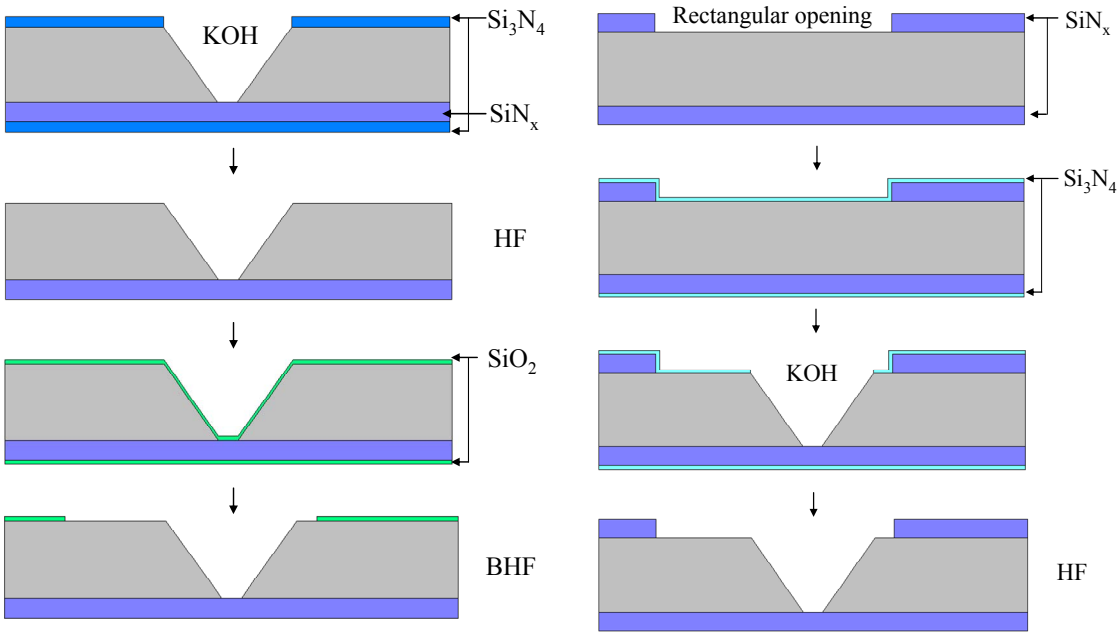

Figure 4.7: Fabrication sequence for device type I (on the left) and type II. For type I after stripping silicon nitride, silicon dioxide is deposited via LTO, and ion implantation region is opened with BHF etching. For type II devices, the rectangular opening is formed by RIE. After KOH etching the silicon nitride layer is released with HF etching.

Once both types reach this stage the back side is patterned using RIE for *p*+ region, and they are sent out for ion implantation. Again As of 15KeV and $10^{15}cm^{-2}$ is used for *n*+ region, and B of 50keV and $10^{15}cm^{-2}$ is used for *p*+ electrode on the bottom.

The rest of the fabrication sequence is identical to the first batch. After the implantation, passivation AR layer is deposited, annealed at 1000°C using RTA (Rapid Thermal Annealing), and patterned for contact. Aluminum is deposited and patterned on both top and bottom for *n*+ and *p*+ contacts. Both types are identical as far as the structure is concerned, except that for the type I devices SiO_2 is used as passivation layer and for type II devices Si_3N_4 is used.

4.2.3 Results and discussion

Figure 4.8 shows a microphotography of the actual photodiode fabricated inside of a pyramidal cavity which is a part of 2×3 array. The square opening is about $450\mu m \times 450\mu m$. As indicated earlier the bottom opening was formed during KOH etching for this set. The outer area is protected by SRSN (silicon rich silicon nitride). The *n*+ implanted arsenic region extends underneath the aluminum contact, a bright rectangular box on the left side. Although it appears to be dark, the sidewall is coated with ~600Å of Si_3N_4 layer as an antireflection layer. This picture also shows some areas, lower right corner of the cavity, where PR failed to cover the edge of the pyramidal cavity during spin coat, and it consequently exposed the silicon nitride layer.

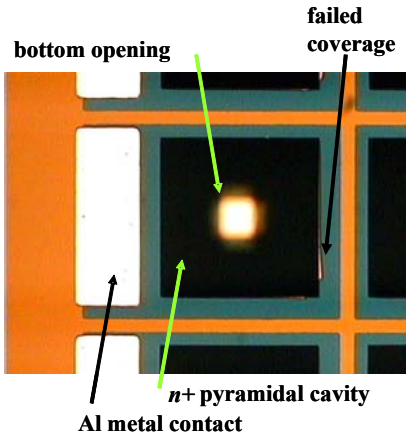

Figure 4.8: picture of a fabricated photodiode inside of a pyramidal cavity.

Unfortunately the fabrication results are not much better than the first batch. Although efforts are made to preserve the bottom dielectric, by the time the fabrication was finished, almost all of them are broken. Figure 4.9 shows one of the better I-V measurements from a type I device. Although the figure may look worse than the previous measurement at a glance, the result is actually better. For this sample the measured dark current is 47.3nA at -10V, and the breakdown occurs at about 45V. (The previous measurements are 500nA at -10V and breakdown voltage of about 30V.)

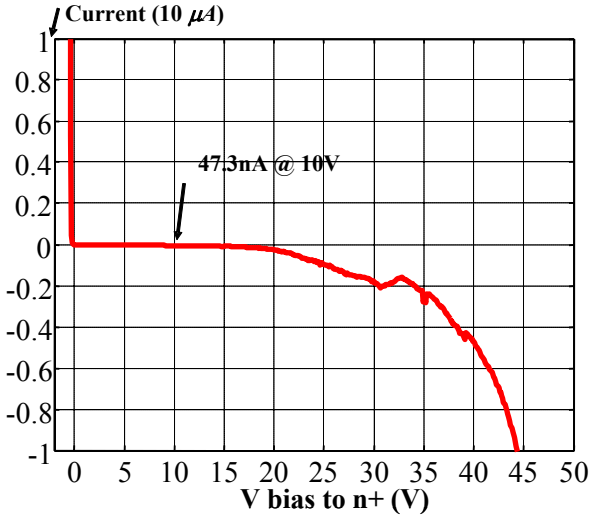

Figure 4.9: I-V measurement of diode fabricated in the pyramidal cavity from the second batch.

On the average the dark current was about 50nA, and for this particular photodiode the commercial chemiluminescent compound is placed inside of the cavity in an effort to measure the photocurrent, which was on average about 54nA. Compared to the first batch the dark current has improved, but it still is far from the desired value of about 0.1nA.

4.2.4 Other findings

During the course of alternating fabrication sequences additional side effects are discovered and are described here. First in the past we have used Si_3N_4 layer as the mask layer during KOH anisotropic silicon etching for creating silicon pyramidal cavities. Nominally about 1000*Å* ~ 1500*Å* of Si_3N_4 was sufficient as the masking layer, but for one of sequences the thickness was increased to over 4000*Å* because the silicon nitride layer also needs to serve as the diffusion and ion implantation mask. It is known that Si_3N_4 layer has internal mechanical stress, and normally a free-standing cantilever fabricated only with Si_3N_4 will not survive the release process. As it turns out thicker Si_3N_4 layer also mechanically fails during KOH etching. Figure 4.10 shows an example of a silicon substrate that starts to show this mechanical failure during KOH etching. Both pictures are from the same substrate. The left picture shows a crack just starting to form where the silicon underneath the crack would be exposed to KOH. The right picture shows what happens under the crack as KOH etching progresses.

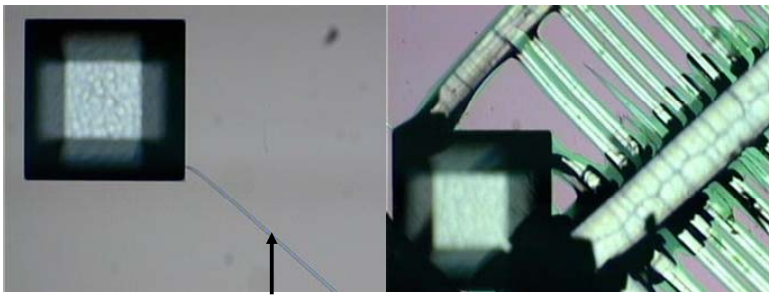

Figure 4.10: Mechanical failure of 4500*Å* thick Si3N4 mask layer during KOH etching.

Additionally KOH etch rate in the <111> plane increase when the region is doped with *n*-type dopants, phosphorous in our experiment. This was observed during fabrication of *n*-type guard ring before forming the pyramidal cavity. Figure 4.11 shows this phenomenon. Initially a long rectangular region is doped with phosphorous ($POCl_3$ 900°C 20min, annealed at 1050°C for about 90min), and the smaller black rectangular region, where silicon is exposed, is etched open. After a long duration of KOH etching (at about 90°C), the light blue region surrounding the black rectangle, over-hanging dielectrics with undercut, is observed. As it can be seen from the picture, the etch rate toward <111> plane within the diffused region is faster resulting in deeper undercut (i.e. thicker light-blue line).

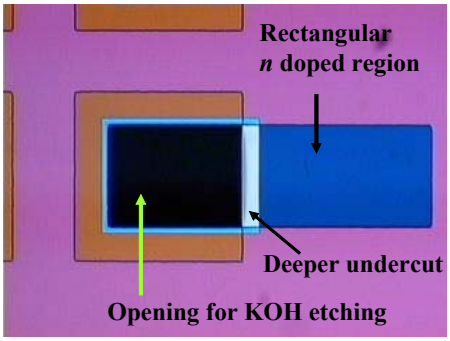

Figure 4.11: A different configuration of photodiode that demonstrates breakdown of <111> barrier in n-type diffusion region during KOH etching.

Apparent explanation of chemical reaction sequence during silicon KOH etching is provided in page 36 of reference [4.4]. It is well known that *p*++ region is etch stop layer for KOH etching, and one of the explanation is the recombination/unavailability of electrons generated during $Si + 2OH^-$. The above phenomenon is in line with this explanation: abundantly available electrons in *n*+ layer enhances etch rate of silicon.

4.3 FOOD FOR THOUGHTS ON DEVICE INTEGRATION

After completing the second batch it became clear that a different strategy was needed. Up to this point the main focus of the integration was concentrated on higher-end of hierarchy so to speak, i.e. how conveniently/efficiently can the fabrication of photodiode be integrated into process flow of fabricating the cavity or how efficient the integrated photodiode can be? More efforts are put into drawing up a complex integration scheme of photodiode inside of the cavity when there was a cover/reflecting layer on top of the cavity like the bead confining layer imagining an integrating sphere like structure. These statements obviously are based on the assumption that a good *pn* junction diode can be fabricated; however, as all the diodes created in both first two batches, perhaps about 10 substrates in total, exhibited unacceptable reverse bias current, the entire integration scheme was revamped concentrating on the front-end of the integration, fabricating a good/sound *n*+/*p* junction diodes.

4.3.1 Standard discussion on degradation of carrier lifetime

As pointed out in chapter 2 significant portion of dark current in silicon *pn* junction consists of generation current, and this generation current is inversely proportional to the minority carrier lifetime. First concerns in standard semiconductor fabrication concerns about minority carrier lifetime are discussed, mostly adopted from reference [4.1] mixed with observations, techniques, and solutions to these concerns.

4.3.1.1 Chemical point defects

It is generally well known that gold is a minority lifetime killer in silicon, and other metallic impurities that fall in this category are copper and iron. They are heavy with higher diffusivity and usually are deep impurities. “During processing, they tend to condense around dislocations so as to form metallic precipitates, which can cause

distortion of the potential lines if they are located in the depletion layer of a *p-n* junction, leading to localized regions of high electric field through which excess leakage current flows" [4.1, p42].

Other than maintaining an impurity free fabrication environment and consistent chemical cleaning of the substrate, gettering is used to remove or reduce defect during semiconductor fabrication. Specifically damage gettering, creating deliberate damages on the back of the substrate away from the active region, is very effective removing/capturing fast moving impurities by providing an infinite supply of sinks during high temperature cycle.

4.3.1.2 Charge states in silicon dioxide

Another factor affecting minority carrier lifetime is charge states in SiO_2. There are two types of charge states: interface traps (fast states) and slow states. As SiO_2 is grown on top of Si substrate, the lattice mismatch between Si and SiO_2 results in interface traps. "Being deep, these traps are responsible for both generation and recombination effects at the surface. Thus, their presence results in increased leakage currents in the region where the junction penetrates to the surface, shorter minority carrier lifetimes, and early falloff in transistor current gain at low levels" [4.1 p477]. A solution is to anneal the substrate after metallization in hydrogen ambient, which forms Si-H bond and reduces trap density. (Although this solution might be temporary as the bond is rather easily broken.)

Slow state occurs from the fact that SiO_2 exhibit positive or negative charge which indirectly influences the electronics below, and the density of slow states can be reduced by growing SiO_2 in dry O_2 ambient at high temperature. Additionally presence of alkali ions such as Na^+, K^+, and Li^+ during the SiO_2 growth also results in *n*-type shift in

surface potential. Both interface traps and slow states play role in reducing the lifetime, which is illustrated in terms of surface recombination velocity [4.1 p480].

4.3.1.3 Dislocations and stacking fault

Other factors during fabrication process that can reduce minority carrier lifetime are dislocations and stacking fault. Dislocation is caused by mechanical stress, which is induced during doping with high concentration or rapid cooling after high temperature process. Stacking fault appears during oxidation on silicon. "The primary effect on stacking fault is that they act as precipitation sites for metallic impurities, which cluster around them in order to relieve stress in the lattice. This, in turn, results in degraded junction characteristics, as well as reduced lifetime" [4.1, p728]. Additional publications which deal with the above problems are reference [4.13-4.16].

4.3.1.4 Examples

This section describes failed experiments, i.e. exhibited excessive junction leakage, during the course of fabrication. For some time all the fabricated *pn* junctions were measured without any metallization, and non-ohmic nature of the contact does show up in forward biased IV measurement. Typically currents are in 0.1mA range at +1V, which translate into about 10kΩ of contact resistance, and for a good *pn* junction, typical reverse biased currents are in sub-nA range which is well over 1GΩ. Therefore it is reasonable to measure reverse biased current without too much concerned about the ohmic contact. At one time a *pn* junction with good dark current in 10's of pA was fabricated; however, after depositing aluminum with E-beam evaporator and patterning, all the junctions showed dark current in μA range. It is not attributed to Kirkendall effect as the junction was very thick and half of the metallized samples were not annealed. It is

possible that the metal evaporated right before this sample, which happens to be gold, may have found its way onto the sample.

During the trial of various recipes of thermal oxidation, one set of samples were left in the oxidation furnace at 450°C in nitrogen ambient for a few hours after growing oxide. Capacitance-voltage measurement of the capacitors built on this substrate suggests that the substrate is *n*-type although the starting substrate was a *p*-type. As it turns out leaving substrates inside of the oxidation furnace long after an oxidation recipe is finished creates sever damage on the surface even if it was in nitrogen ambient. This was confirmed with other students who experienced the same phenomena, and the behavior is very similar to description of slow states.

4.3.2 Fabricating *pn* junction diode using phosphorus diffusion

Before fabricating a photodiode within pyramidal cavity efforts are made to fabricate a planar *n*/*p* junction diode. $POCl_3$ (Phosphorus Oxychloride), a liquid phosphorus diffusion source, is used to create *n* region instead of ion implantation for the following reasons. First MRC (Microelectronics Research Center) at University of Texas at Austin does not have ion implantation capability, and it took roughly 2~4 weeks of turn around time for outsourcing although faster turn around time was desired and needed. Additionally ion implantation creates damage on the surface which could degrade electronic performance; specifically it is more difficult to remove/anneal these damages for heavily doped shallow regions. [4.1] RTA activations step following the implantation turns out to be problematic as well from time to time as the fabricated wafers have cavities etched all over, and half of the wafers would either crack or melt during RTA cycle. Finally one of the initial design is as mentioned to integrate a cover layer, a cantilever, to contain as much of photon inside of the cavity as possible. Obviously if most of the sidewall is hidden underneath the cantilevers is would be

impossible to create $n+$ region using ion implantation; whereas it might be possible to do so with phosphorus diffusion.

First a thermal oxide (both wet and dry) was grown on top of silicon wafer. After protecting the back side with PR squares are patterned on the other side and etched onto SiO_2 with BHF. After striping the PR wafers are diffused with phosphorus, the back side SiO_2 was stripped, and IV curve was measured without metallization. (Non-ohmic contact would show in forward biased condition, but it really should not matter for reverse biased measurement. As the primary objective at this point was to reduce the dark current, metallization was skipped.) Oddly enough only about 25% of the samples, wafers to wafers, showed good reverse bias currents. Wafers with good reverse characteristics exhibited 10's of pA; whereas poor wafers showed reverse biased current in μA. Here is another odd example. After wet oxidation, patterning, and phosphorus diffusion, the wafer was cut in half, and the back oxide was removed only in one half. Both halves are then annealed at 1000°C for 5mins. As it turns out the piece with removed back always showed significantly better dark current. (One set showed about 100pA versus 2~3nA)

4.3.3 DSP vs. SSP (Gettering)

A significant amount of time was spent to figure out why many of the simple *pn* junctions exhibited excessive dark currents for no apparent reasons. Different combinations of fabrication conditions, i.e. wet or dry oxidation at different temperatures, are tried to pin point the cause or develop a good recipe. As it turns out most of the junctions/devices created at this institution are fabricated on a SSP (single side polished) wafers. If all the conditions are perfect, i.e. the furnaces are free from ionic contamination or perfect oxidation recipe with precise thermal control ability (ramp up and ramp down), it really should not matter whether the substrate is DSP (double side polished) or SSP. If

the purchased wafers are perfect, i.e. very low oxygen content or high purity with long minority carrier lifetime, again it really should not matter. But obviously the world is not perfect, and the author believes that the rough back side of SSP wafers might have played a gettering role during thermal processes.

References [4.5~4.8] deals with different gettering techniques as well as how defects specifically oxygen precipitation defects can raise junction leakage currents and how they may be removed by intrinsic gettering. The point is by removing/gettering the source of defects on the surface longer carrier lifetime can be achieved in turn achieving better device performance. This actually brings up an interesting question. In order to fabricate any electrical device inside of a KOH etched pyramidal cavity, the cavity has to be etched through/toward the bulk of the substrate. Intrinsic gettering, for example, creates a "denuded zone" at the surface by annealing the substrate and move the oxygen toward the bulk. First this technique can only be done in an oxygen free environment; otherwise, oxygen would simply diffuse into the surface. Second if intrinsic gettering technique is to be used, it would have to be carried out after the cavity is etched. Otherwise the oxygen drove into the bulk of the substrate would likely to be exposed during formation of cavities. Unfortunately the thermal furnaces in MRC are not perfect. For example when a substrate is placed inside of an annealing furnace at high temperature, the silicon substrate was tined indicating that a finite layer of SiO_2 is grown although the annealing was carried out in N_2 ambient.

Damage gettering, placing mechanical damage on the back of the substrate on purpose before thermal process, is adopted for this project. These mechanically damaged regions are supposed to attract impurities during thermal process. Although it is not clear if not fabricating devices on a SSP is the cause of the failure as gettering is a secondary

effect, most of the junctions fabricated with this mechanical damage on the back showed good reverse bias characteristics whereas ones without it did not.

4.3.4 Carrier lifetime

As described in earlier section gettering technique is related to maintaining or improving minority carrier lifetime by removing defect, reference [4.9] for example. By maintaining a good minority carrier lifetime a low dark current can be achieved. References [4.17-20] have excellent discussions on various reports of measured minority carrier lifetime for different substrates along with mobility/diffusivity and some physical explanation as well as numerical predictions on minority carrier lifetime.

4.3.4.1 Si_3N_4 vs. SiO_2 (substrate thickness)

Earlier in the first two batches Si_3N_4 is used as starting dielectric layer. As it turns out this can cause serious damage to the silicon substrate with irreversible effect on reduction of minority carrier lifetime, and apparently this is well known in solar cell community. Reference [4.10] well illustrates this point by measuring minority carrier lifetime after depositing and removing LPCVD silicon nitride. Silicon nitride is required as the masking layer during KOH etching. Although some literatures indicate that SiO_2 can be used as the masking layer, in the authors experience this simply is not true: all SiO_2 deposited with LPCVD LTO, grown in wet or dry at high or low temperatures exhibited significant etch rate with warm KOH. For this project silicon nitride with extra DCS is exclusively used as silicon rich silicon nitride has lower stress and provides good protection of substrate during KOH etching [4.11].

Moreover the thickness of the wafer that is used for electronic taste chips is about 250~300μm, which is about half of the normal thickness used in conventional microelectronics. It is logical to think that for whatever reason when strain or stress is

applied to the substrate, the mechanical effect or damage on thinner wafer would be twice as much. (Even SiO_2 has internal stress, about 1/3 of the stress applied by silicon nitride.) One explanation of this stress is mismatch in the TEC (Thermal Expansion Coefficient), and limiting and maintaining a low thermal budget is another strategy taken in hopes of applying less stress on the substrate and maintaining the minority carrier lifetime. Additionally thermally grown SiO_2 should provide better passivation and lower surface leakage current compared to SiN_x.

4.3.4.2 Measuring generation lifetime

Efforts are made to measure generation carrier lifetime by fabricating a square MOSCAP and by applying and measuring voltage pulse to the capacitor. Figure 4.12 shows diagrams explaining the pulsed MOSCAP method and graphs of ideal responses, obtained from reference [4.12]. When the capacitor on a *p*-type substrate is biased with negative voltage, V_g, holes accumulate underneath the metal electrode, and the measured capacitance consist only of the capacitance formed around the dielectric, C_{OX}, which is phase I in the figure. When V_g is suddenly changed to positive, initially a deep depletion is formed near the interface, phase II, and then minority carriers are generated, in this case electrons, and attracted to the electrode until equilibrium, phase III. By measuring the time, t_f, generation rate can be extracted.

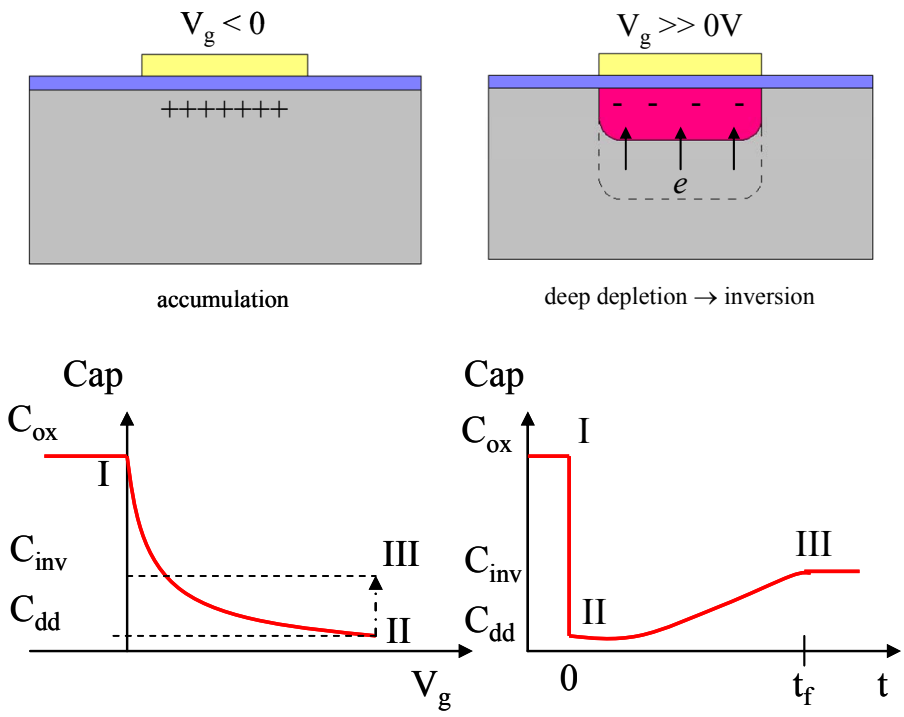

Figure 4.12: Diagrams illustrating the pulsed MOSCAP method and ideal C-V and C-t response.

Figure 4.13a shows two C-V curves from two different samples, one with only wet oxidation after KOH etching and the other with a combination of thermal oxidation: a thin layer of dry oxide with chlorine at 950°C for 1 hour followed by annealing at 1075°C for 5min, and then wet oxide at 950°C for 50min. Although both samples are cleaned with RCA cleaning, the CV curve of substrate with only wet oxidation shows a shift in V_{FB}, which indicates poor interface or ionic contamination. This measurement was made in the process of testing dry oxidation with TCE. As suggested in reference [4.1] dry oxidation with TCE is deposited at lower temperature followed by annealing at above 1050°C which should improve minority carrier lifetime. Figure 4.13b shows the C-t response, where the dots are the actual measured values and the line is the fitted curve

for the capacitance. The generation carrier lifetime can be estimated by pulsed-MOSCAP method, which is used to obtain the slope of Zerbst plot (Figure 4.13c) using the equation from reference [4.12] (C_{ox}~70pF and C_{inv}~26pF),

$$-\frac{d}{dt}\left(\frac{C_{ox}}{C}\right)^2 = \frac{2n_i}{\tau_{g,eff}N_A}\frac{C_{ox}}{C_{inv}}\left(\frac{C_{inv}}{C}-1\right)+\alpha \quad (4.1)$$

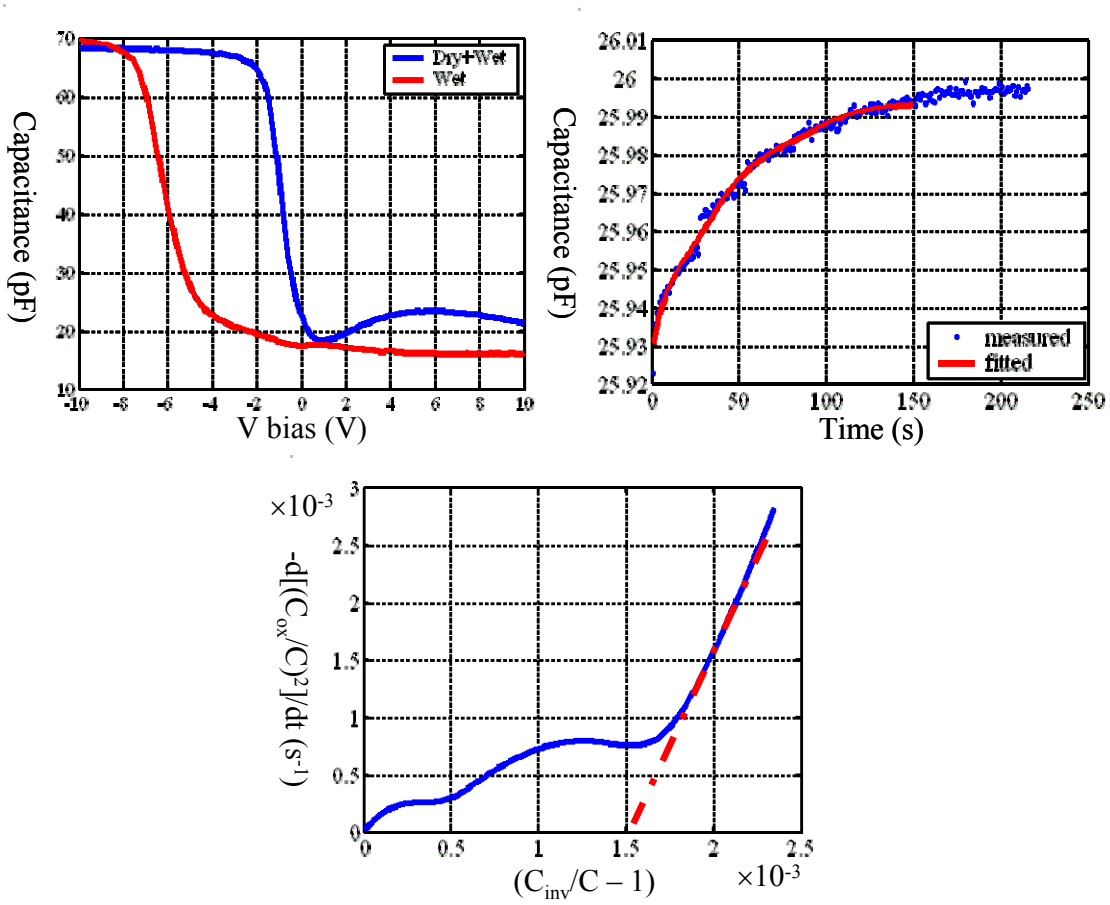

Figure 4.13: C-V plot, C-t plot, and Zerbst plot obtained from MOSCAP of the processed substrate.

For this particular sample, the generation carrier lifetime was estimated to be about 15μs, and the generation current is estimated to be about 93pA at -10V, which is

about twice larger than target dark current, obtained from $A \times qn_i W/\tau_g$. Dry oxidation with TCE at 950°C for 45mins followed by annealing at 1075°C for 20mins is used throughout as initial passivation layer directly on top of silicon.

4.3.5 Conclusion

During the course of investigating what would cause the excess dark current, first possible effect of damage gettering is considered. This thought has evolved to maintaining substrate quality, i.e. minority carrier lifetime, during the bulk micro-machining. The fabrication sequence has been simplified and separated reflecting these thoughts: first the required cavity is fabricated with the consideration of maintaining the minority carrier lifetime, and second the photodiode is fabricated with limiting thermal budget.

4.4 REVAMPED FABRICATION SEQUENCE

Two integration processes with slightly different fabrication sequences have been completed. One process is based on the same CZ grown silicon substrate used in the previous sections. The second process is based on neutron doped FZ grown silicon wafers which as it turns out, are about the same price as the CZ grown wafers for double side polished (DSP) custom thickness substrates.

4.4.1 Integration process using CZ Si wafers

First a thin layer of thermal wet oxide is grown at 950°C for 15 minutes, and this is followed by deposition of a SRSN (silicon rich silicon nitride, LPCVD 820°C DCS:NH_3~2.5:1) layer. The gas ratio was chosen so that the nitride film has relatively low stress and is also relatively easy to wet etch at later stage using HF acid. The square opening that will ultimately determine the size of the storage well is patterned and etched with RIE (CHF_3:O_2~8:1 at 150W), and the cavity is etched using KOH. For these

experiments the KOH etching was terminated after etching about half way through the substrate for convenience in later stages of fabrication. Right after the KOH etching, a modified SC-2 cleaning is carried out for decontamination of K^+. The wafers are submerged in self boiling solution of HCL, H_2O_2, H_2O (~1:1:1) for 5 minutes, rinsed and dipped in BHF for 5sec, and then etched in poly-Si etchant for 1 min. The above steps are repeated 4 times except the last step was replaced with complete removal of previously deposited films using 49% HF.

Before growing a fresh layer of thermal oxide, the back side of the wafer was mechanically damaged, and the wafers went through a traditional RCA cleaning cycle. A thin layer of dry oxide with chlorine is grown at 950°C for 60 minutes followed by annealing at 1075°C for about 5 minutes. An additional layer of wet oxide is grown for about an hour at 950°C, and a large rectangle is patterned and etched using BHF on top of the opening. The $n+$ active region is formed with $POCl_3$ (phosphorus oxychloride) at 900°C for 10 minutes, the oxide on the back is etched, and Al is evaporated on top and bottom. The substrates were then annealed at 450°C for 5 minutes in forming gas. Although each deposition layer and steps have been changed, most of the masks used in this experiment are the same ones used in the first two batches.

4.4.2 Integration process using FZ Si wafers

As pointed out earlier neutron doped DSP FZ grown silicon wafers with lower resistivity (2~3Ω-cm) cost about the same as DSP CZ grown silicon wafers. Since the doping concentration is higher and minority carrier life time is much longer (guaranteed to be >1000μs), the generation current, which is the major source of dark current in silicon diodes [2.20], should be much smaller because of shallower depletion width and longer generation carrier lifetime. At the same time the quantum efficiency would be smaller due to the shallower depletion width. With these expectations in mind, a slightly

altered fabrication sequence has been developed using the same patterns used with the diodes discussed above. The fabrication steps before the second thermal oxidation are identical to the CZ case, including the damage on rear surface. After the RCA cleaning the same thin dry oxidation step with TCE is carried out. However, for the neutron doped DSP FZ substrates a guard ring was to be fabricated with shallower active region; hence, a much thicker oxide was needed. To reduce the thermal budget a LPCVD LTO (~535°C) was used to deposit this thicker oxide. These steps are illustrated in figure 4.14.

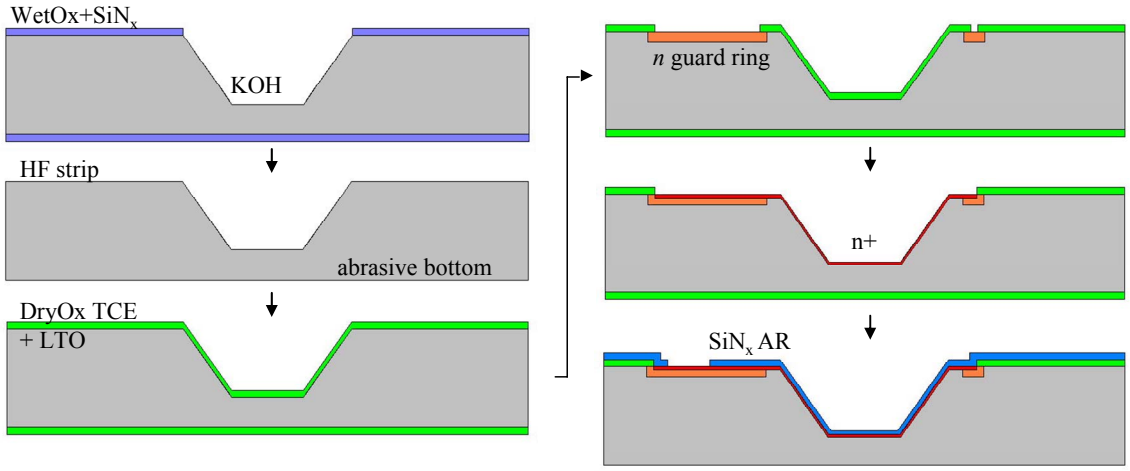

Figure 4.14: Diagram of fabrication sequence for the FZ substrate. The sequence for CZ based fabrication is a simplified version of this sequence.

About 1μm of SiO_2 was deposited on top of the dry oxide. A guard ring was patterned and etched with BHF around the top opening of the cavity, and *n*-region was created with $POCl_3$ at 900°C for 20 minutes followed by drive in at 1000°C for 20 minutes. Afterwards the oxide on top of the cavity was removed with a smaller rectangular pattern, and an *n*+ active region was created with $POCl_3$ at 900°C for 7.5 minutes. Additional silicon nitride layer was deposited to act as an anti-reflection (AR) coating between liquids to be placed in the wells and the silicon photodiode. In addition a

contact opening on top of the guard ring region away from the active area was made using RIE, and the dielectrics on the back were removed.

4.5 RESULTS AND DISCUSSION

Figure 4.15a shows a current voltage (IV) curve measured for a typical diode fabricated using this process on a CZ wafer. As indicated in the figure the dark current was significantly reduced to -0.5nA at -5V. The measured photocurrent is about -1.4nA. The top opening was slightly larger, but the overall volume of the cavity is identical for the old and new photodiodes. Figure 4.15b shows the IV curve of the FZ devices. For this particular sample at the time of writing, substrates had not yet been processed through final metallization. Electrical testing without this final metallization, however, has been performed. As expected the dark current of -74pA at -5V is much less than that of the diode fabricated on a CZ substrate. On the other hand the photocurrent generated with roughly the same amount of the same chemiluminescent sample is about -0.5nA at -5V, compared to about 1nA produced by the CZ diodes; however, the ratio of photocurrent to the dark current for FZ substrate is larger than that of CZ substrate. The breakdown (reverse biased current reaching 10μA) for the FZ substrate occurred at about -41V.

Although samples were not metalized it should not hinder the electrical measurement. Tungsten probed is poking $n+$ region, and mechanically damaged bulk is held down on a brass vacuum chuck. For all the samples measured current in forward biased conditions showed about $0.1mA$ to $1mA$ at +1V, indicating that the non-ohmic resistance is about 10kΩ at most. For devices with good reverse biased characteristic the dark current is less than $1nA$ which translates into 1GΩ; therefore, metallization would be unnecessary at least in reverse biased conditions.

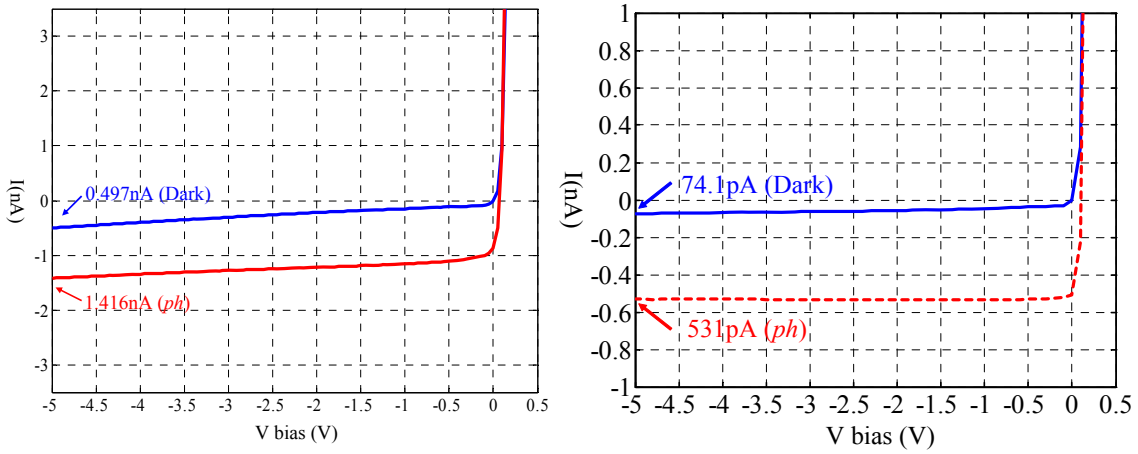

Figure 4.15: Measured IV curves of photodiodes integrated within silicon pyramidal cavity. a) on the left is measurement made on CZ substrate. It shows decent dark current of -0.5nA with photocurrent of -1.4nA from ~20nL of chemiluminescent sample. B) on the right is measurement made on FZ sample.

The doping concentration of $n+$ region would be close to solid solubility limit for phosphorus, and electrically active concentration is about $5\times10^{20}cm^{-3}$ diffused at 900°C. [4.1] Doping concentration for the FZ wafer is estimated to be $10^{16}cm^{-3}$, and using the standard equation depletion width is estimated to be $0.36\mu m$ at equilibrium and $0.95\mu m$ at -5V. Using the generation current equation the generation lifetime for this FZ device can be estimated to be about $60\mu sec$, and similarly $25\mu sec$ for devices on CZ wafers with depletion width of about $3\mu m$.

Chapter 5: Performance

This chapter describes the fabrication issues and measured performance of the last devices fabricated within cavity. Minor alteration of the fabrication flow is presented as well as the description of the experiments.

5.1 FINAL PRODUCTS

5.1.1 Fabrication flow on CZ wafer

The overall fabrication flow is identical to the one presented in section 4.4, and some minor alteration is described here. As it turns out the devices fabricated without the initial oxidation step worked just as well; therefore, the first oxidation step was not carried out and simply replaced with piranha cleaning without removing the thin oxide layer that grows during the cleaning. The DCS flowrate for LPCVD silicon nitride layer is slightly increased so that overall 40% of 100sccm DCS and 5% of 300sccm ammonia is used to deposit 1000$\mathring{A}$ of SiN at 800°C. Finally $POCL_3$ doping is carried out at 800°C for 5 minutes instead of previously used 5 minutes or 90 seconds at 900°C for doping active region. This should decrease the junction depth even further making the photodiode more efficient.

Right after the second phosphorus diffusion photoresist is applied on the front and the oxide on the back is etched with mixture of BHF. Adding about 10% in volume of HF acid enhances the etch rate without damaging the photoresist. There is some oxide grown on top of the junction during diffusion, and the probe is landed directly on top of it. Measurements are made after biasing the probe with high forward biased voltage of 20V to break the dielectric. Additionally landing the probe inside of the cavity, making the same measurement, and comparing the dark current assure that the junction is created within the cavity and is electrically connected to the guard ring/probing area. Figure 5.1

shows an IV curve of the diode measured right after the diffusion on a CZ substrate. Although there are some glitches near -1V, the dark current measured at -5V is about 50pA. The breakdown voltage is about 73V.

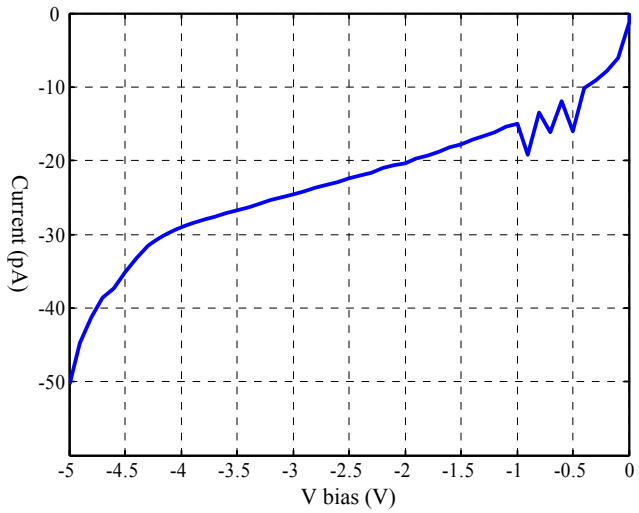

Figure 5.1: measured IV curve on CZ substrate after phosphorus diffusion of 5 minutes at 800°C.

The 50pA is the smallest dark current observed of a shallow junction fabricated within the cavity on a CZ wafer. After making the electrical measurements the wafer is cleaned with piranha cleaning and LPCVD is used to deposit silicon nitride AR coating. After the deposition of the AR coating contact opening are made on the front via photolithography and RIE. The backside silicon nitride layer is also removed with RIE. At this stage IV curve is measured again, but unfortunately the same cavity, which the above measurement is made, showed dark current in excess of 1nA.

Following reasons are possible cause for sudden increase in the dark current, relating to the earlier discussions on the parameters affecting the dark current. First as the wafer goes through this additional thermal cycle it is possible that the interface between thin SiO_2 and silicon has changed creating additional defects or traps. The wafer could

have been contaminated with impurities that reduce minority carrier lifetime. Although the same furnace is used to deposit the first silicon nitride layer, wafers go through cleaning, silicon delineating etching, and dry oxidation with chlorine steps which have been known to increase the minority carrier lifetime.

Another possible explanation is that a part of active $n+$ region might have been exposed during RIE. Figure 5.2 shows picture of a completed device, one of the samples that were actually measured. One of the constant challenges in creating the device was photolithography step after the cavity has been etched. Although HMDS oven is used to coat the wafers with adhesion promoter before spin coating photoresist, the edges around the top openings are almost always peeled off exposing a part of $n+$ region, connecting to the n guard ring. Similar issues as well as comparing with solutions such as spray coating photoresist is well documented in reference [5.1].

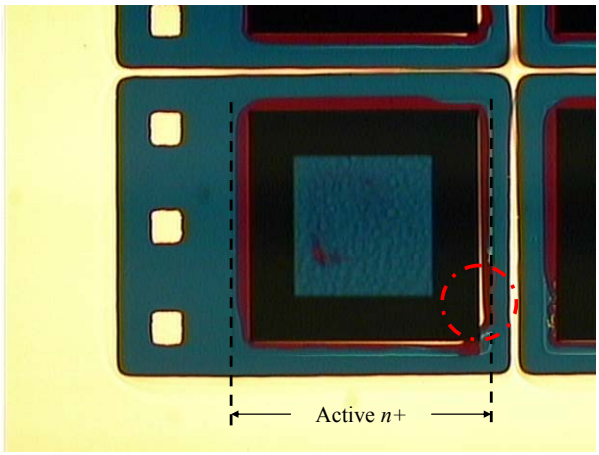

Figure 5.2: picture of photodiode fabricated within cavity illustrating photoresist not covering up the side of top opening properly. This is the cavity that was actually measured for the IV curve in figure 5.3.

Fortunately one of the other cavities retained a decent dark current of about -0.25nA, and although it is much higher than -50*pA*, it is smaller compared to the CZ device introduced in chapter 4. Figure 5.3a) shows the IV curve measured from device pictured in figure 5.2, and b) shows transient response of the same device biased at -5V. The breakdown after depositing LPCVD silicon nitride has moved from -73V to about -84V.

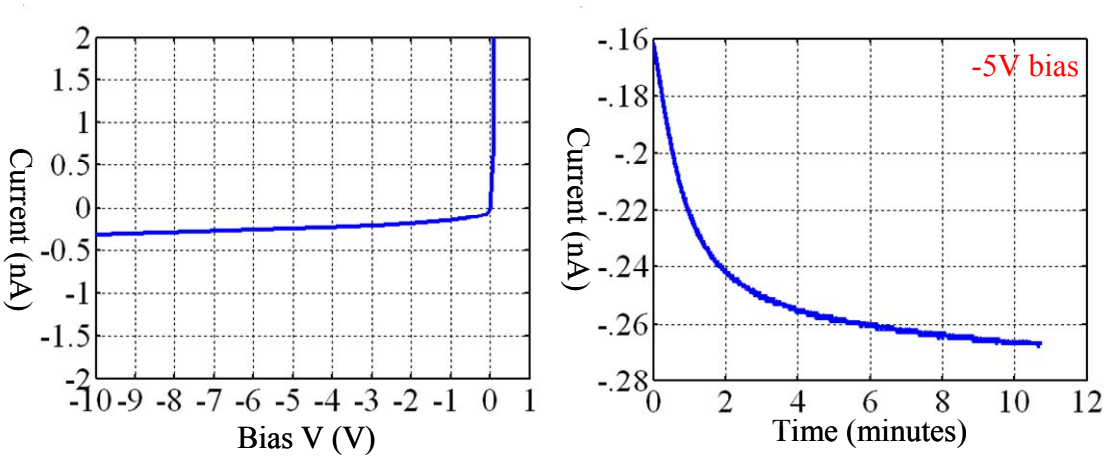

Figure 5.3: IV curve and I-t curve of diode within cavity on a CZ wafer coated with LPCVD silicon nitride layer.

5.1.2 Fabrication flow on FZ wafer

The fabrication flow for the FZ sample is identical to the CZ sample, except after the active diffusion AR coating is deposited with PECVD. The advantage of PECVD is that the deposition temperature, 250°C, is significantly lower than that of LPCVD system, and the junction depth should be shallower. On the other hand the index of refraction is somewhat lower as the film is less dense, and this results in higher reflectivity at target wavelength. Also exposing silicon during deposition may result in surface damage as it is assisted by rf plasma. Additional process related advantage of PECVD silicon nitride is that the film is very easily etched with BHF; therefore, during

the contact formation the opening is simply etched with BHF which should not affect silicon underneath. PECVD silicon nitride layer is deposited with 2sccm of NH_3, 150sccm of N_2, and 100sccm of SiH_4 at 250°C and 900mTorr under 20W of rf power. These FZ wafers showed even lower dark current compared to the FZ wafers presented in chapter 4 with LPCVD AR coating. Before depositing PECVD silicon nitride layer the dark current was about -6pA, and after the dark current rose to about -10pA. Figure 5.4 shows both IV curve and I-t curve at -5V before and after PECVD nitride coating. Breakdown voltage has shifted from -43V to -47V.

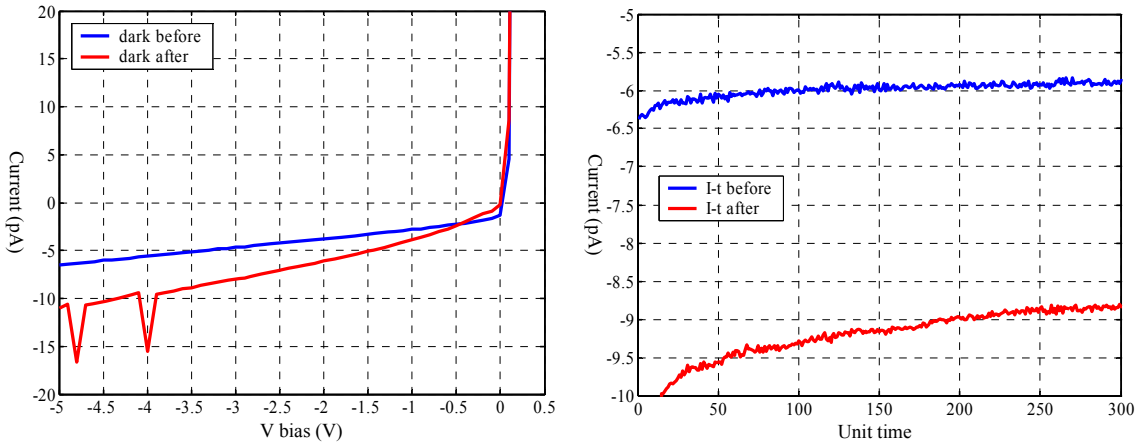

Figure 5.4: Dark current IV curve of FZ wafers before and after PECVD nitride deposition and the same transient response at -5V. Unit time is about 0.2 seconds.

5.1.3 Discussion

The device fabricated on FZ wafer has superior electrical characteristics. It does have smaller dark current, but more importantly the transient response is much more stable compared to that of the devices fabricated on CZ wafer. A commercial silicon pn junction photodiode from Hamamatsu, S2506-02 [5.3], is used as the bench mark, and figure 5.5 shows the dark current measurement made on S2506.

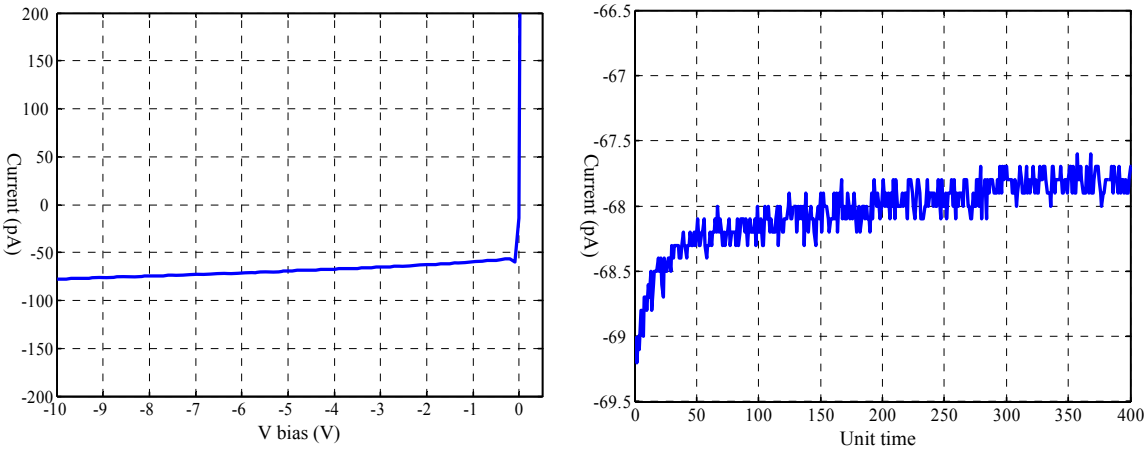

Figure 5.5: Measured dark current response of Hamamatsu S2506. Unit time is about 0.2 seconds.

The dark current at -5V bias is -69.3pA, and roughly the area of S2506, 2.77mm×2.77mm, is about ten times larger than the fabricated photodiode. The dark current density for S2506 at -5V is -9×10^{-10}A/cm^2. The dark current of FZ device with PECVD AR coating is -9.94pA, and the surface area is about 5.6×10^{-3}cm^2, which results in the dark current density of about -18×10^{-10}A/cm^2. As far as the dark current is concerned this really is not a bad number considering that the commercial photodiode would have been fabricated in a dedicated clean environment; however, to be fair in comparison, most of the area on S2506 is active region whereas only about half of the surface area is the active region on the fabricated diode. (The other half is used as the guard ring/contact area.) On a side note the dark current density of CZ wafers is about -450×10^{-10}A/cm^2, which is about 50 times larger than S2506.

5.2 QUANTUM EFFICIENCY

5.2.1 Setup

Efforts are made to roughly measure the quantum efficiency of the fabricated photodiode. As the interested wavelength of optical communication group is either 1.3μm or 1.6μm, the light source in visible range is not readily available. Best option would have been to acquire a laser at the interested wavelength so that the light can be aimed at inside of the cavity, but laser at 500nm is also not commonly available. Some of the requirements for making this type of measurement are to have light source with known wavelength, maintain constant distance between the light source and the target, deliver the light to known area, calibrate the light or flux, and replicated the same condition during the measurement of the interested device. On top of these requirements, for making wafer level measurements, electrical connection also needs to be considered.

At the end mounted LEDs with collimating lens were purchased as the light source from Thorlabs, Inc. [5.2] Two LEDs, MGLED and MRMLED, are purchased, and they have wavelength of 530nm and 455nm with optical power of 90mW and 240mW, respectively. A 2inch hole is drilled on a 6inch by 6inch 1/8inch thick aluminum plate to mount the light source, and this is placed on top of the metal frame that holds the microscope. The distance between the light source and the probe station should be constant, and efforts are made so that the lateral position of the light source was also the same between each measurement by aligning two edges of the aluminum plate to the end of the frame. The relative position of the device is kept track of by maintaining the lateral position of the tungsten probe tip. Figure 5.6 shows picture of this setup inside of the shielding metal box.

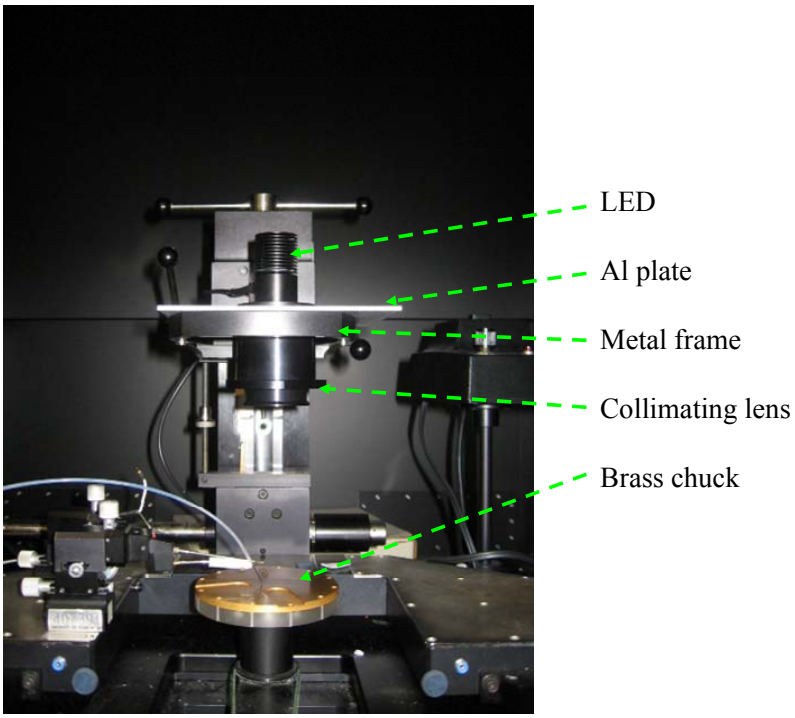

Figure 5.6: Setup for measuring quantum efficiency.

For each measurement the wafer is placed on the brass vacuum chuck, and the contact is made with the tungsten probe on the small square in the middle shown in figure 5.2. Additional challenge to making such measurement is isolating the photodiode so that the photo current is not induced from unwanted area. In order to accomplish this a photo-etched thin brass piece with roughly $1060\mu m \times 430\mu m$ opening is used to cover the photodiode. After determining the position of the tungsten probe, the tip is raised and the shadow mask is placed and aligned to the device by hand. The probe tip is lowered again, and the electrical connection is verified. After positioning the shadow mask the microscope is detached from the frame, and the mounted LED is placed as shown in the picture. The photocurrent is measured on the fabricated device, the probe tip is raised again, and the wafer is removed. Right after removing the wafer, the commercial

photodiode is placed on the brass chuck and positioned relative to the probe tip so that the active area of the commercial photodiode, which is about 10 times larger than the diode in testing, covers the area where measured device was. The shadow mask is placed again on top of the commercial photodiode, and the photocurrent is measured. Figure 5.7 shows the spectral response of the commercial photodiode, directly captured from the specification sheet [5.3], and this graph is used to tabulate the optical power.

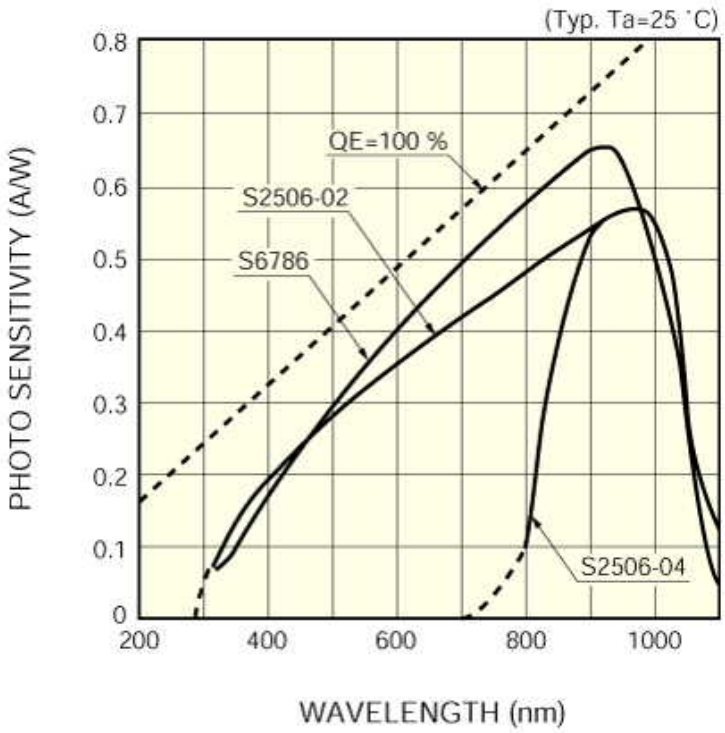

Figure 5.7: Spectral response for S2506 silicon pn photodiode from Hamamatsu [5.3].

The light source appears to be reasonably in this simple setup. After picking a position with the tungsten probe, one corner of the S2506 was focused/targeted with the probe tip, and photocurrent is measured without any shadow mask. Then the other corner is targeted by moving the photodiode, i.e. measured 4th quadrant and then moved the

diode to measure 1st quadrant while tungsten probe is stationed in between 2nd and 3rd quadrant. The measure photocurrents were 24.1μA and 24.3μA.

5.2.2 Measurements

Table 5.1 lists the measurements made with the method described in the previous section. The measurement is carried out in room temperature with -5V biasing. There are two values for S2506 measurements because each is taken with respect to the position of the samples measured. The dark current at this point is excluded as they are significantly smaller than the measured photocurrents.

	FZ / S2506 (μA)	**CZ / S2506 (μA)**
455nm	**1.11 / 1.96**	**1.14/1.51**
530nm	**0.586 / 1.14**	**0.591/0.809**

Table 5.1: measured photocurrent of fabricated photodiodes.

Table 5.2 shows the translated photo sensitivity of each fabricated diode at the two wavelengths. Figure 5.6 is opened with Adobe Illustrator, which has built in ruler, and the efficiency of S2506 is read off as 0.25 for 455nm and 0.38 for 530nm. To put these numbers in perspective, quantum efficiency, obtained by $R \times 1240/\lambda$, is written next to the sensitivity in parenthesis.

	FZ (A/W)	**CZ (A/W)**	**S2506 (A/W)**
455nm	**0.14 (38%)**	**0.19 (52%)**	**68%**
530nm	**0.20 (47%)**	**0.28 (66%)**	**89%**

Table 5.2: Extracted responsivity and quantum efficiency.

5.2.3 Discussion

At this point the sensitivity of the fabricated photodiode is not as good as S2506. As pointed out earlier photodiode fabricated on FZ substrate is expected to have lower quantum efficiency because the doping concentration of the substrate is about one order of magnitude higher than the CZ wafer,2~3Ω·cm vs. ~25Ω·cm; therefore, it is no surprise that FZ wafers showed less efficiency in the above table. Additionally in general it is more difficult to detect lights at lower wavelength especially near UV because more photons are absorbed near the surface; hence, much thinner junction is needed to detect more photons at the wavelength. From the very beginning the device is designed toward detecting lights at 500nm, and although the above response may be natural, i.e. better efficiency because of longer wavelength, it is encouraging that both fabricated diode indeed showed better efficiency at 530nm. However the measured quantum efficiencies are somewhat conservative values. Some compromises had to be made in order to make the electrical connections to the photodiode, and guard ring region, which is about ¼ of the shadow mask, where efficiency is not as great are exposed during measurement. Figure 5.8 illustrates this point.

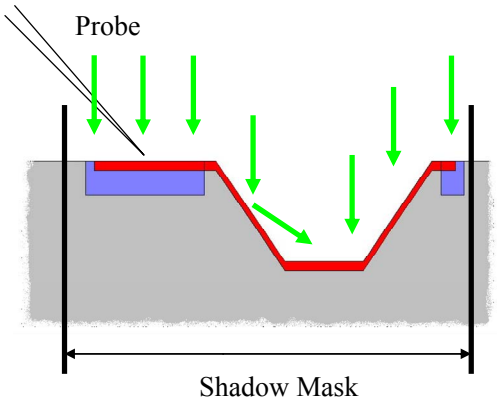

Figure 5.8: Illustration of factors affecting QE measurement.

Additionally about half of the light is hitting the sidewall, meaning that the incident angle is about 55° and reflectivity is close to 50%. The reflected light would likely to hit another portion of the cavity, but the overall effect is very complicated. During the measurement the shadow mask is moved (to left in figure 5.8) so that it covers most of the cavity/active region. The photocurrent generated from this setup was about 10% of the measure photocurrent indicating that about 90% of the measure photocurrent is from active region.

5.3 DETECTING LIQUID CHEMILUMINESCENT COMPOUND

5.3.1 Setup

Efforts are made to calibrate the amount of liquid chemiluminescent compound that induces photocurrent within the cavity. A mechanical dispenser, which is supposedly capable of dispensing 1nL, is purchased from KD Scientific. [5.4] The model number of purchased pump is KDS101 infusion pump, and in order to dispense nano-liters of liquid 10μL syringe, which is not readily available in local medical supply stores, is required. 10μL syringe is purchased from Hamilton [5.5] along with 22 gauge needle and plastic tubing for the diameter. The purchased model is Gas Tight 1701 syringe with removable needle.

For the application the conventional manipulator of tungsten probe is converted so that a spare needle with sharpened tip is glued on instead of the tungsten tip. This needle is connected to the syringe with the plastic tubing. A seal was created at the each end of the tubing using epoxy, and later it was reinforced with thin cyanoacrylic glue. During the dispense chemiluminescent compound is sucked through the manipulator tip, the excess compound outside of the tip is wiped off, the tip is guided toward the cavity, the liquid is dispensed, and the tip is raised before closing the metal box for the

measurement. During the guiding and dispensing the movement as well as dispensing is observed through the microscope. Figure 5.9 shows a picture of this setup.

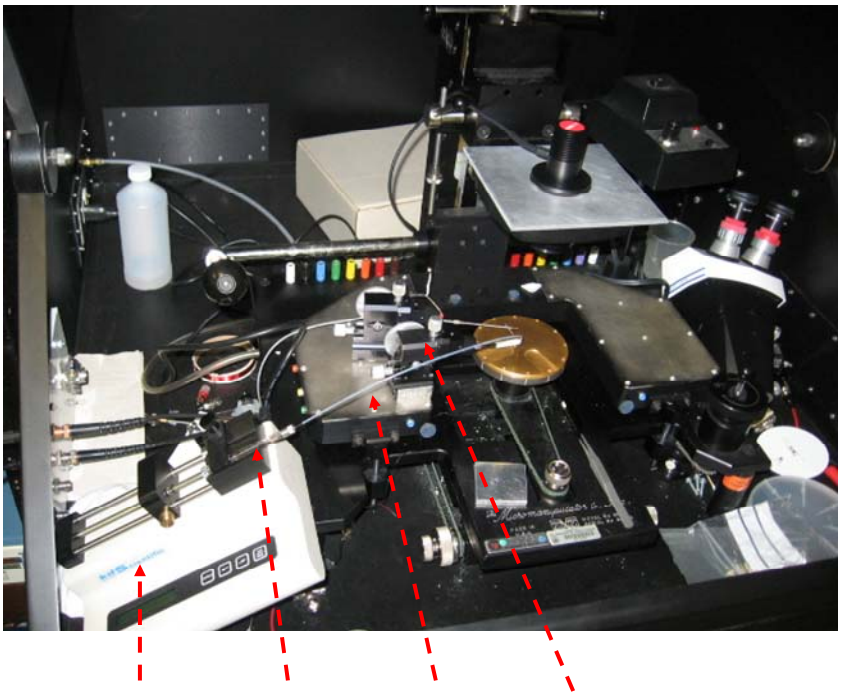

Figure 5.9: picture of the setup for liquid dispenser.

5.3.2 Problems

The setup described above did not work too well. First the syringe is not sturdy enough to actually draw $10\mu L$ through the needle and tubing in consistent manner. The needle attached on the manipulator is shorter than the needle attached to the syringe; therefore, the chemiluminescent compound should be visible through the clear plastic tubing near the manipulator tip if the full amount was extracted through the manipulator tip. This has happened only in a few occasions. This would also explain why half of the times the liquid does not come out through the tip while the machine is trying to move

the lever to dispense 20nL. Second in a way this is a bit more severe problem, the dominant force that controls/influences the liquid sample appears to be not the syringe but rather capillary force formed between the cavity and the needle. Most of the time nothing happens as the pump is trying to dispense 20nL. On the occasion when some liquid does come out, as soon as the tip is lowered touching the cavity, the cavity completely over flows with the chemiluminescent sample, i.e. additional liquid inside the tip is drawn out, virtually making the measurement useless. In an effort to minimize this effect, a different needle with knife-like edge is created, which also turns out to be fruitless.

In the earlier samples a sharpened wire with a nick has been used to pick up the chemiluminescent compound by hand. The wire is then lowered toward inside the cavity, and as the tip touches the cavity, the cavity is filled with the compound. As it is very apparent, as shown in figure 5.10, whether the cavity is under filled, ideally filled, or completely overfilled, this type of delivery is used for measuring chemiluminescent response. When it is ideally filled the bottom edges/corners are clearly visible from the top, and the spot in the middle of the cavity for under filled case is part of the bottom surface. It would be impossible to tell whether the volume of liquid is 19nL or 21nL, but as shown in figure 5.10, it probably is less than say 30nL.

Under filled Ideal

Figure 5.10: Pictures of 20nL cavities under/ideally filled with liquid.

5.3.3 Measurements

Figure 5.11 shows I-t measurement of the FZ and CZ cavities filled with the commercial lightstick compounds. For these measurements the starting photocurrent was about 1.6nA for FZ sample and 2nA for CZ sample. The unit time is about 0.2 seconds.

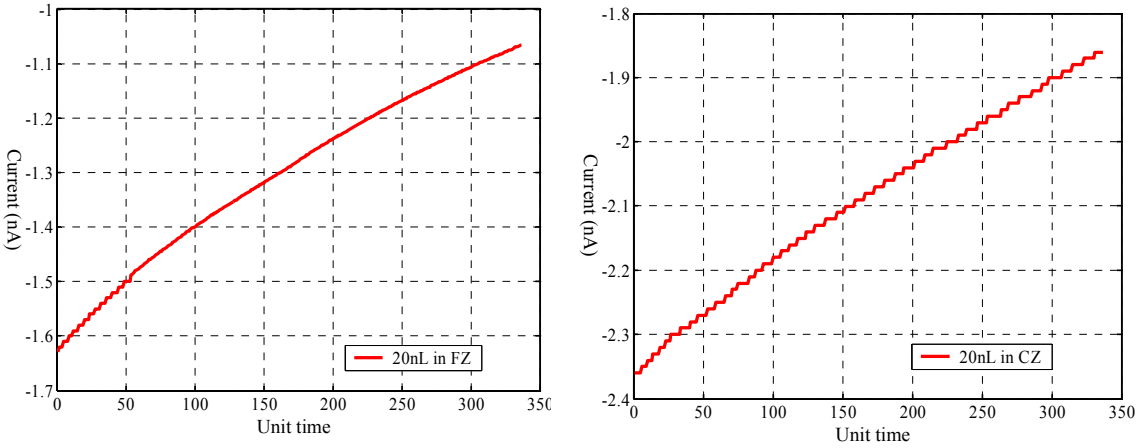

Figure 5.11: I-t measurements after filling the cavities with chemiluminescent compound.

5.3.4 Discussion

First it is apparent that the number of photons emitted by the commercial sample drops rather rapidly. From the FZ sample the detector is collecting about 1.6nA worth of photons, which means that, using the responsivity obtained earlier, the chemiluminescent sample is generating about 8nW or 2×10^{10} photons. Although the rate rolls off the response shows that roughly 0.1nA worth of photons (1.3×10^{9}) are diminishing in 50 unit time or about 10 seconds. Although it is highly unlikely that the time to fill up the cavity and start the transient measurement will be different for over a minute between each measurement, variance of at least a few seconds not if tens of seconds, which translates into 0.01nA to a few 0.1nA, should be considered. Looking at the CZ sample the initial

2nA translates into 7.1mW or 1.9×10^{10} photons, which happens to be different from the FZ case of about 1×10^{9} photons.

Comparing these results with earlier results presented in chapter 4, following conclusions can be made on the different diodes fabricated on different substrates addition to the discussion made earlier. The FZ substrate presented in this chapter showed almost similar efficiency as the CZ wafer presented in chapter 4. In fact the performance gap between CZ device and the FZ became smaller because active region created at 800°C for 5 minutes is shallower than one created at 900°C, and this effect is carried over as the FZ sample has PECVD coating rather than LPCVD coating carried out at 800°C for about 45 minutes. (Simple $(Dt)^{1/2}$ arguments would show the junction depth is about 1/3.) PECVD nitride, however, should be about 10% less efficient in absorbing photons due to lower index of refraction.

Another way to interpret the result is to calculate the minimum detectable concentration. For the FZ devices roughly 20nL chemiluminescent sample has generated about 1.6nA of photocurrent. Since the maximum dark current is about 15pA setting the minimum detectable current for this system to be 1.5pA, 10% of the dark current, translates into minimum detectable volume of the same compound to be about 0.02nL. If the minimum detectable photocurrent is 1.5pA it is equivalent to about 10^{7} absorbed photons per second. If we assume that the QE is about 50% at 500nm the minimum detectable number of photon from the luminescence becomes 2×10^{7} per second. If the quantum yield of commercial light stick is assumed to be 20%, the number of reacting molecules generating 2×10^{7} photons would be about 1×10^{8}. Numerically 1×10^{8} molecules in 20nL of a solution is equivalent to 5×10^{12} molecules/cm^{3}, and this is equivalent to about 8×10^{-9}M.

5.4 NOTES ON THE COLLECTION EFFICIENCY

As demonstrated in the previous section the manner of how the light is collected can heavily influence the overall performance of a photodetector. In this section this discussion carries over even further by considering flow of the liquid delivering the sample to the cavity. Number of discussions on the micro-fluidic aspect of such deliveries can be found in literatures such as references [5.6, 5.7, and 5.8].

5.4.1 Basic equations

For a semiconductor photo detector, the photocurrent generated by light with energy greater than the band gap can be approximated by

$$I_{ph} = q \times carriers/\sec = q \times \eta \times photons/\sec = q \times \eta \times A_{diode} \times (\frac{photons}{A_{diode} \cdot \sec}),$$

where q is the electronic charge, *carriers* are the number of holes and electrons generated within and around a diffusion length of the transition region participating in generating the photo current, η is quantum efficiency, the ratio of number of carriers generated from the available number of *photons*, and A is active area of the detector. Hence the photocurrent is directly proportional to the number of available photon, and if the source of the illumination happens to be a fluidic medium, the number of available photons per unit time is further influenced by

$$\frac{photons}{\sec} = QY \times \frac{molecules}{\sec} = QY \times N_{concentration} \times \frac{Vol}{\sec},$$

where QY is the quantum yield, term used in chemistry indicating the ratio of number of photons generated to the number of reacting molecules, and the number of molecules can be estimated by the concentration of the molecule within the volume of the fluid.

Obviously, the performance of the detector itself, i.e. a higher η, is always important; however, what is equally significant, especially when the detected is a fluid, is to actually have the photons or molecules available and supply/deliver them to the detector within specific time. It is very likely that the limiting reagent would be the target analyte, and the "supply/delivery" can be quantified as *Vol/sec* or flow rate.

5.4.2 Geometry

Now the geometry starts to play a role, and in order to estimate the flow rate for a microfluidic structure, equation describing the behavior of an orifice is considered. C_D is the discharge coefficient, which is the ratio of actual flow rate to that of a theoretical flow rate, and is defined as

$$C_D = \frac{Q}{A}\sqrt{\frac{\rho}{2 \cdot \Delta P}} \quad [5.7],$$

where Q is the flow rate, and A is the opening area of an orifice, ΔP is the pressure drop across the orifice, and ρ is the density of incompressible fluid.With all the constants and efficiencies set aside, referring to figure 5.12, I_{ph} is proportional to the opening area, D^2, and I_{dark} is proportional to the surface area, D×L, if the detector is built on the side wall of the orifice. Therefore I_{ph}/I_{dark} is proportional to D/L.

First of all the interested wavelength of the light generated by chemiluminescence is in visible range, and in particular, our system generates around 500nm light, a green color. Water has very low absorption coefficient (α) around that wave length, and one of the higher absorption coefficient reported at 500nm is about 0.06cm^{-1}. Using the Beer's law, $P_{out}=P_{in}e^{-\alpha z}$, where z is the length of penetration, P_{out} drops to 99% when z is 1675μm! When z is 5000μm, P_{out} drops to about 97%. Hence, the intrinsic absorption

loss in aqueous medium at the interested wavelength is quite small. Second, a simple argument can be made based on the geometry. Figure 5.12 shows a cross section of an orifice.

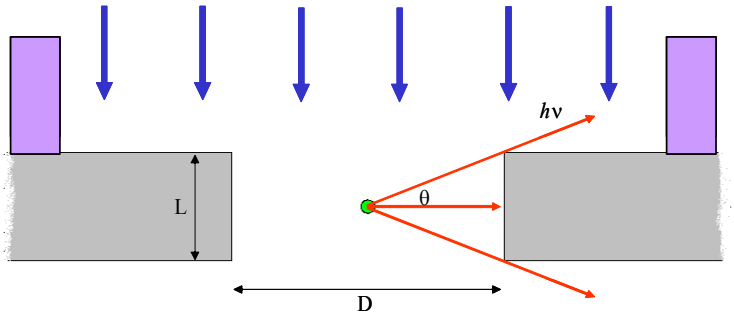

Figure 5.12: illustration regarding the case when a photon is generated in the center of an orifice.

If we assume that a photon is generated at the center of the orifice, it has chance to start off to any direction, 360°. The angle which the photon would be hitting the side wall can be expressed as $\theta = \tan^{-1}(L/D)$. Therefore the probability of the photon actually hitting the sidewall would be $4\times\theta/360$. By combining the absorption loss and geometrical loss, I_{ph}/I_{dark} is proportional to

$$\frac{I_{ph}}{I_{dakr}} \propto e^{(-0.06\times\frac{D}{2}E-6)} \times \frac{4\tan^{-1}(\frac{L}{D})}{360} \times (\frac{D}{L}).$$

Figure 5.13 shows the plots for the above equation with a) variable D with fixed L of 300μm and b) variable L with fixed D of 100μm. As the diameter of the orifice gets larger, I_{ph}/I_{dark} increases because the total number of photons available grows with the flow rate. When the diameter reaches about 2000μm, the ratio starts to saturate due to less number of photons reaching the side wall (geometrical effect), and in fact, starts to decline as the absorption start to take effect. Similar interpretation is applied to the effect

of variable L. As the length of the orifice, i.e. thickness of the substrate increases, the flow rate is reduced, and I_{ph}/I_{dark} decreases. And simply there is less number of photons to influence I_{ph}/I_{dark} with geometrical effect and absorption for large L.

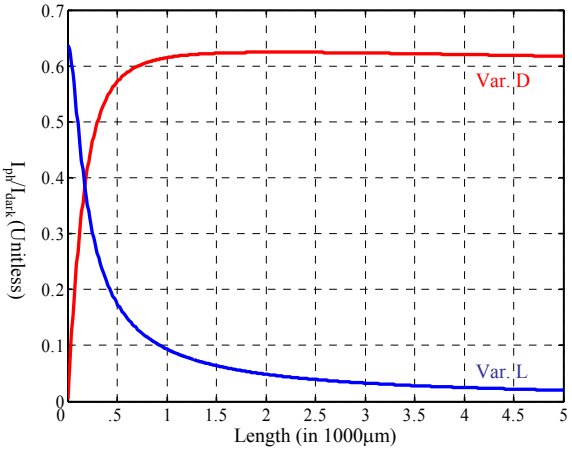

Figure 5.13: Effect of varying L or D on the ratio of I_{ph}/I_{dark}.

Figure 5.14 is 3-dimensional graph of varying both D and L at the same time. Figure 5.13 would be a 2-dimensional slice of this graph when D or L is a constant.

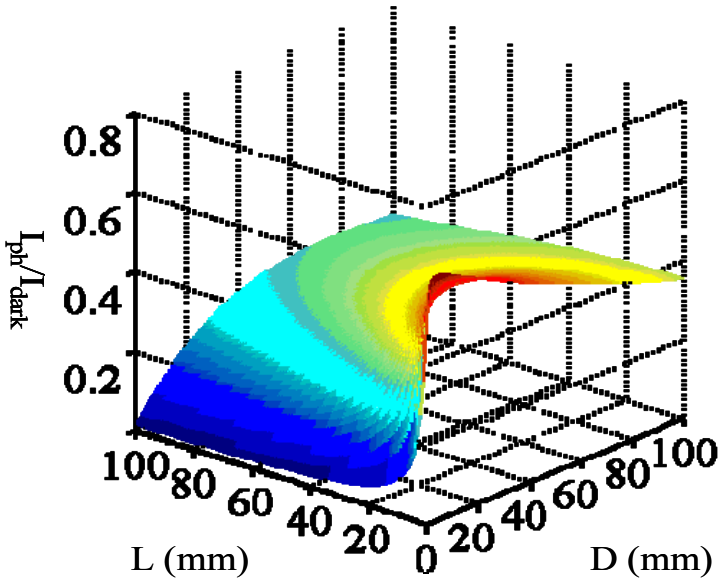

Figure 5.14: 3 dimensional graph of I_{ph}/I_{dark} with variable D and L.

5.4.3 Emission rate vs. flow rate

Another factor that would affect determining the geometry would be how the sample is flown through the detector. The experiments in this project are carried out in an ideal environment. A stable chemiluminescent source is used which has everlasting high emission rate; therefore, the sample is simply dropped on top of the detector and analyzed. This is a case of "stopped flow," where the delivery of sample is well controlled, and the only concern is the emission rate of the sample at a given moment. In this case the analysis in section 5.4.2 would be valid. However in real life it is highly unlikely that the detected target would be controlled. It would be more like the sensor would have to detect whatever the life throws at it, and in that case both the emission rate and flow rate should be considered in designing the sensor.

If the emission rate is much higher than the flow rate, then the dimension would not be critical. At any given moment there will be enough photons coming off from the sample, and one extreme example would be sunlight. In fact the other extreme example of higher emission rate would be the stopped flow, flow rate = 0.

On the other hand if the emission rate is slower than the flow rate, then it can be problematic. For example if one photon is generated in 10nL of sample in 1 second, that 10nL of sample better stay within the detector for at least 1 second in order to get a chance to absorb it. If the flow rate is fast enough, 20nL/s for example, so that it takes less than a second to pump 10nL through the detector, the probability of grabbing the photon would decrease. Then diameter needs to be smaller hindering the flow rate or the length need to be longer to retain larger volume. Unfortunately both solutions are against the trend of obtaining higher I_{ph}/I_{dark}.

5.5 EXPERIMENT WITH HYBRID ON PASSIVE RFID READOUT

5.5.1 Assembly and measurement

After fabricating the photodiode within the micromachined silicon cavity a rapid prototype of "tag" circuit was assembled to test the passive RFID readout. For the transmitting coil a commercial EAS tag, a tank circuit consisting of a spiral inductor and a capacitor, is disassembled by soaking it in a lacquer thinner, and the spiral inductor is extracted by removing the capacitor. After cleaving one set of 2×3 array on a silicon wafer the photodiode is attached to the inductor using conducting silver epoxy. A wire is used to connect the aluminum contact on the top to the end of the inductor. The entire structure is glued on a plastic plate, and the inductance is approximately 4μH. Figure 5.15 shows a picture of this hybrid prototype.

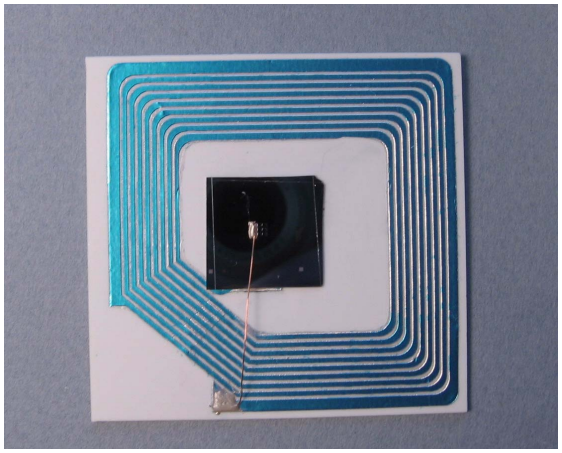

Figure 5.15: A picture of the hybrid prototype consisting of the fabricated photodiode, extracted spiral inductor, and a wire connecting the two using conductive silver epoxy.

After the assembly this prototype is interrogated using another wire connected to impedance analyzer HP4149A. Figure 5.16 shows magnitude and phase response of the input impedance of this reader coil.

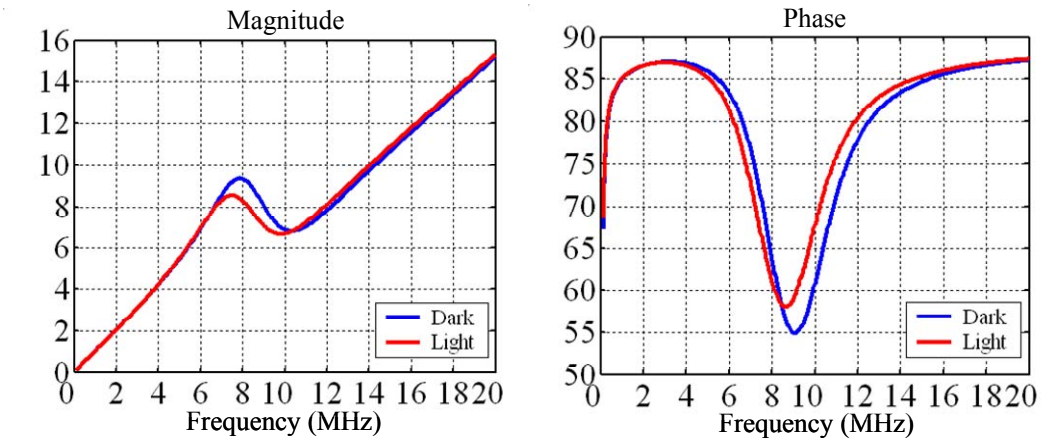

Figure 5.16: Magnitude and phase response of the hybrid prototype.

Unfortunately the measured response is not as good as the earlier example presented in chapter 3. The width of the phase dip is wider, and all the corners of the phase response plot are not as sharp. More importantly the device is not as sensitive to light, i.e. the small change in resonant frequency in figure 5.14 is induced not by chemiluminescent sample but by a much brighter microscope light source.

5.5.2 Discussion

5.5.2.1 Structural difference in PIN diode and pn diode

The poor response of hybrid prototype built with fabricated photodiode may be attributed to the inherent difference in the structure of silicon PIN photodiode, the commercial example in chapter 3, and silicon *pn* photodiode, the fabricated photodiode in the cavity. As the name implies PIN diode has an artificial near-intrinsic region created in between *n*+ and *p*+ layer; therefore, regardless of the DC bias condition the thickness of the depletion region should remain fairly constant whereas the thickness of the depletion

region of *pn* diode strongly depends on the DC bias condition. For the fabricated photodiode the depletion width, calculated with standard equation for doping concentration of $N_A=10^{15}\ cm^{-3}$ and $N_D=10^{20}cm^{-3}$, is estimated to be $1\mu m$ under 0V and $3\mu m$ under -5V bias. Roughly speaking the photodiode used in passive RFID readout is biased at 0V, and the number of EHPs generated within depletion region obviously would depend on the thickness of the depletion region. As the fabricated *pn* photodiode is geared toward operation under DC reverse biased condition it may just not be efficient enough to be used as main transducer of passive RFID-type readout compared to PIN photodiodes.

5.5.2.2 Difference in the circuit response

The structure of PIN diode and *pn* diode is different, and naturally the small signal model for PIN diode and *pn* diode is different. As pointed out earlier the small signal model of PIN diode is capacitor and resister in series, and the small signal model of *pn* diode is capacitor and resister in parallel. Ideally a pure capacitive load modulated by light would show ideal response as illustrated in the basic circuit analysis done earlier. In this section presence of resistive element at the load in series or parallel to the capacitor is discussed. Figure 5.17 shows two tag circuits in consideration: a) model for PIN diode and b) model for *pn* diode.

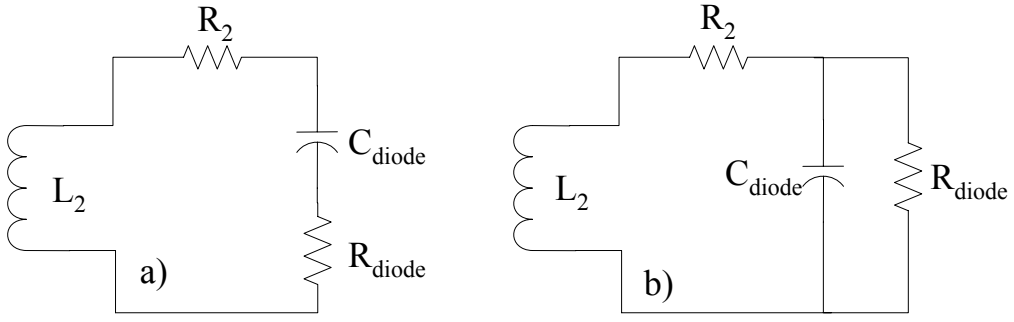

Figure 5.17: Tag circuit model for a) PIN diode load with capacitor and resister in series and b) pn diode with capacitor and resister in parallel.

Conceptually to achieve ideal AC response the resistive element should be as small as possible for PIN diode, i.e. short, and the resistive element should be as large as possible for *pn* diode, i.e. open. Figure 5.18 shows two graphs of calculated input impedance of the reader coil for the above tag models. Both coils are set to be 4μH's, resistance of coils, R_1 and R_2, are set to be 1Ω's, coupling efficiency of 50%, and both C_{diode} = 200pF with varying R_{diode}.

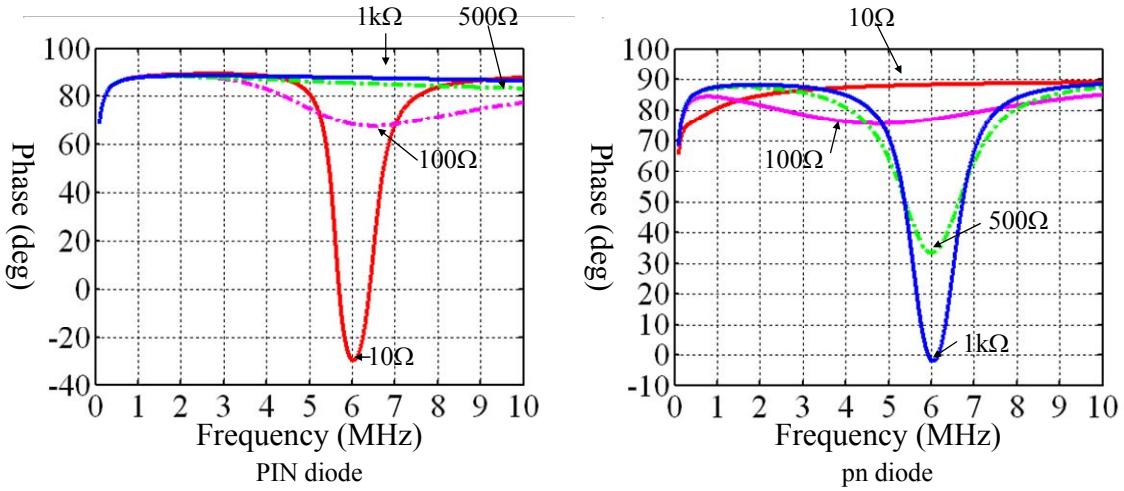

Figure 5.18: Calculated phase response of reader coil input impedance when a) resistive load is in series with capacitor and b) resistive load is in parallel with capacitor. For both cases R_2 is varied from 10Ω to 1kΩ.

It is clear that calculated response illustrates smaller resistance results in sharper phase dip for PIN diode and bigger resistance for *pn* diode. Moreover the resonant frequency is affected by value of the resistance. For PIN diode resonant frequency/phase dip is not apparent when R_{diode} is 500Ω or larger, and the phase dip is located at higher frequencies. On the other hand for *pn* diode the phase dip occurs at lower frequencies for smaller resistance. For both cases there is no dip for biggest/smallest resistance. Figure 5.19 shows similar calculation when a capacitor is placed in series. First the resonance

shifts to higher frequency as extra capacitance is present in the tag circuit, and more importantly in both cases the phase dip appears to be sharper. For PIN diode with external capacitance the difference in resonant frequency with different resistance is smaller, i.e. ω_c (10Ω with external cap) - ω_c (100Ω with external cap) = 0.38MHz but ω_c (10Ω without external cap) - ω_c (100Ω without external cap) = 0.48MHz. This indicates that external capacitance minimizes the effect of change in resistance in series. This effect was reversed for *pn* diode, i.e. the difference in resonant frequencies with or without external capacitance is slightly larger.

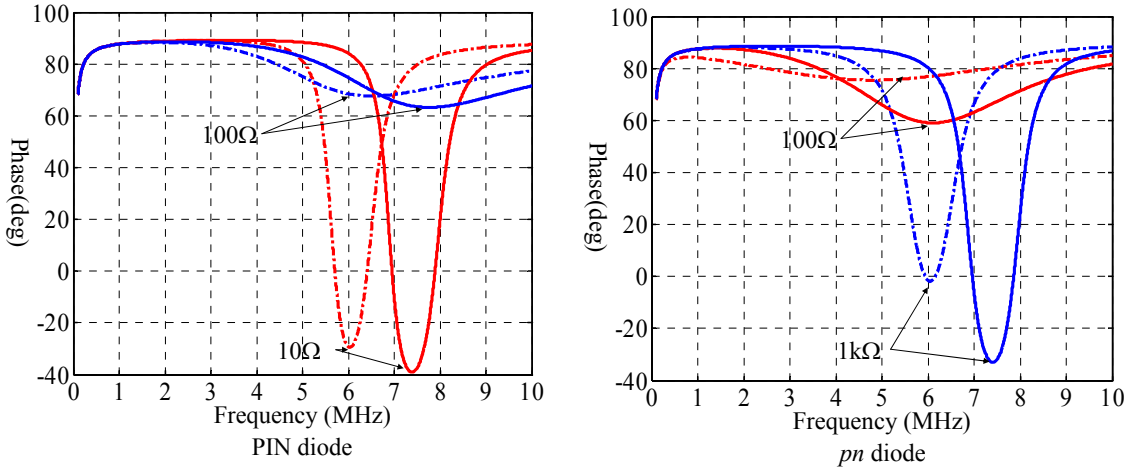

Figure 5.19: Change in the phase response when a capacitance of 400pF is placed in series to PIN and *pn* diodes.

5.5.2.3 Qualitative discussion on tag circuit

From the above examples the external elements of the tag circuit clearly affects the overall response of the sensor. In this section qualitative analysis on effects of different external circuit configuration on the two diode configuration is presented. Figure 5.20 is a block diagram illustrating the permutation. One thing to keep in mind is that the capacitance and resistances of the photodiode is not separate elements but the electrical characteristic of one device, and they are interrelated. The capacitance and

resistance depends on the design of the photodiode, i.e. increasing the area of the photodiode would results in larger capacitance and smaller resistance.

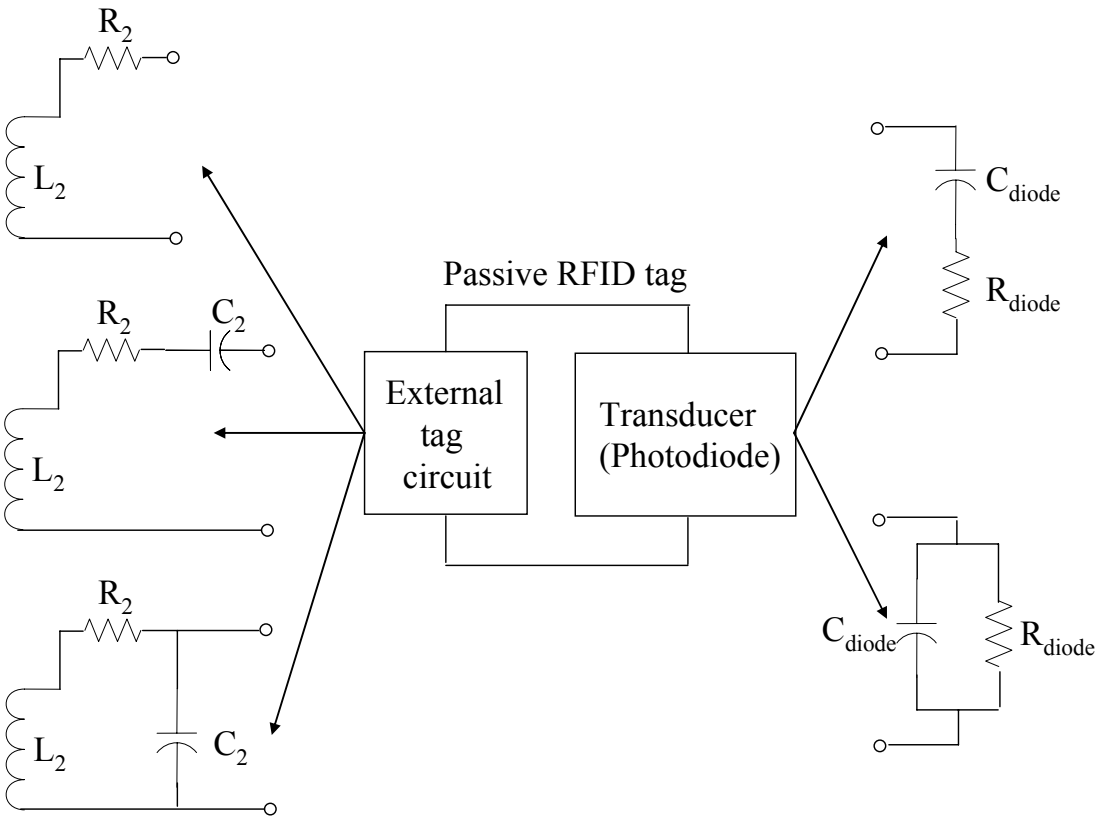

Figure 5.20: Block diagram illustrating possible configuration of passive RFID tag when photodiode is used as the main transducer.

Additionally when the photodiode is illuminated the capacitance increases and the resistance decreases, and this is apparent in figure 5.21, measurements made on one of the fabricated photodiode within the cavity. Without any external connection, i.e. measuring the diode in short circuit mode, the measured values are changing from point

A to point B in figure 5.21. The DC bias of figure 5.21 is labeled as unit V because there was significant contact resistance through silver epoxy used to glue the connections.

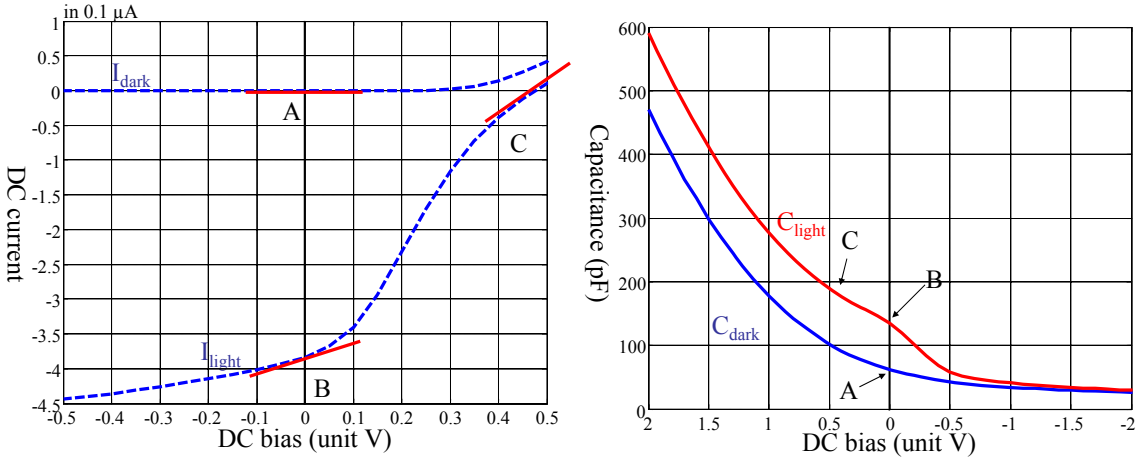

Figure 5.21: Measurement made on the fabricated photodiode within cavity under dark and under illumination. On the left shows DC IV response and on the right shows CV measurement.

Analysis carried out in the previous section is the two simplest configuration of RL external tag, top left corner in figure 5.20, with PIN or *pn* diode. As shown in the previous sections R_{diode} significantly affects the AC response. If the value of R_{diode} is reasonable, i.e. small enough for PIN diode or large enough for *pn* diode, the phase dip shows up, and the resonant frequency is determined by L_2 and C_{diode}. Hence the location of the phase dip will shift depending on the change in C_{diode} but this will again only be recognizable with reasonable R_{diode}. Another possible scenario for PIN junction is that R_{diode} in dark is too large to show phase dip but in light is small enough to show resonance. For *pn* diode R_{diode} in dark may be big enough to show resonance but becomes too small under illumination so that the phase dip disappears.

For the third tag circuit when a capacitor is attached in parallel to the diode, it really should not affect the overall behavior. Specifically when the diode is illuminated, it

acts like a DC current source, and capacitor acts like an open circuit. It simple moves the phase dip toward lower frequency due to additive capacitance in parallel. The calculated impedance does suggest that phase dip becomes slightly sharper.

More interesting phenomenon occurs for the second case when a capacitor is connected in series to the diodes. When a capacitor is connected in series, there cannot be any DC current flowing through the tag circuit. Only logical explanation is that generated charges will be stored in the external capacitance, and this in turn is like placing a DC bias on the diode, point C in figure 5.18 where DC current is 0A. Comparing the points A, B, and C, decrease in resistance as well as increase in capacitance becomes greater.

Chapter 6: Conclusion and Future Work

This project, a part of MEMS-type chemical sensor known as "Electronic Taste Chip," started out as to integrate optical detection mechanism directly on an array of micromachined silicon pyramidal cavities, reminiscent of a microplate, by doing so currently required microscope optics as well as CCD camera imaging the reaction occurring within individual cavities can be eliminated, and the chemical sensor can be used out side of conventional laboratory settings which can be a paramount advantage in many situation. After the consideration of different types of optical detectors and various possible integration scheme the most straight forward/practical approach was to fabricate light sensitive *n+/p* photodiodes directly onto the sidewalls of the pyramidal cavities as the chemical reactions would be occurring right next to the cavity.

Initially the fabricated photodiodes within cavities exhibited very large dark current in DC reverse bias which is the foremost basic merit of sensitivity. Key to fabricating *pn* junction with small reverse biased current appears to be maintaining as grown minority carrier life time during the fabrication of the cavity because bulk of the dark current is generation current which strongly depends on the generation carrier lifetime. After numerous classical literature research fabrication technique geared toward creating junction with low reverse biased current and integrated with fabrication within/after forming the cavity has been devised.

n+/p junction within cavity on a Float Zone (FZ) wafer exhibited dark current of about 10*pA*, biased at -5V, translating into dark current density of about 2×10^{-9}A/cm^2. This dark current density is very comparable to commercially available planar *pn* junction photodiode and also translates into generation carrier lifetime of about 1*msecond*! On a side note the dark current density of *n+/p* junction fabricated within

cavity on Czochralski (CZ) wafer is about $45\times10^{-9}A/cm^2$, which is about 50 times larger than that of commercial photodiode. This dark current density translates into generation minority carrier lifetime of about $10\mu second$, and generation carrier lifetime measured using MOS capacitor made only with thermal oxidation and metallization on CZ wafer was about $15\mu second$. This suggests that the minority carrier lifetime after undergoing the entire fabrication sequence on CZ wafer is very close to as grown minority carrier lifetime, and the devised fabrication sequence has met the initial objective of creating *pn* junction within cavity with low reverse biased current.

Both photodiodes are examined further for its optical characteristic of detecting chemiluminescent reaction occurring within the micromachined cavity. At this time of writing the quantum efficiency, 66% on CZ wafer at wavelength of 530nm under -5V bias, is not as good as the commercial *pn* photodiode with quantum efficiency of about 89% at the same wavelength. However the 66% is a conservative number because the collimated LED light source was illuminating the junction from the top, meaning majority of the light was absorbed with incident angle of 54°, which will result in lower absorption. Additionally the guard ring surrounding the cavity, which should have very low efficiency, was part of the optical measurement.

Another part of the project was to investigate the accessibility of a photodiode via wireless passive RFID-type readout. This is a novel approach because normally a photodiode is operated in DC bias condition measuring DC current, but RFID-type readout is measuring the change in capacitance and AC resistance of the *pn* junction. The potential advantage is the enhanced portability as well as more convenient access of the photodiode operating in aqueous medium. First the commercial photodiode is used to successfully demonstrate the idea, and this initial response is analyzed. Next a hybrid prototype using the fabricated photodiode within cavity is created. Although the rapidly

created prototype using photodiode built for low dark current in DC reverse bias condition was not as good as the initial demonstration, possible explanation for the poor response is presented, and based on the explanation guidelines and design consideration for passive RFID-type readout of photodiode is presented.

There are a number of possible future works based on this project. One of the initial designs was inclusion of overhanging/reflecting cantilever covering most of the cavity so that the entire cavity becomes its own integrating sphere. Hence the collection efficiency will be enhanced even further. Another possible work is to adopt PIN diode rather than *pn* junction photodiode. This can be achieved by growing near intrinsic epitaxial layer after creating the cavity on silicon wafer. If clean/defect free surface can be maintained then achieving artificial depletion region with better electrical characteristic compared to CZ wafer might be possible. Finally additional work can be done on the passive RFID-type readout by designing and fabricating dedicated photodiode for this purpose as the initial demonstration showed promising result.

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Vita

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